KMDA-2631

User's Manual

Ver.A0.1

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Product Warranty (2 years)

JHC warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by JHC, or which have been subject to misuse, abuse, accident or improper installation.

JHC assumes no liability under the terms of this warranty as a consequence of such events.

Because of JHC.s high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an JHC product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Please consult your dealer for more details.

If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU speed, JHC products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an RMA (return merchandise authorization) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from JHC. Please contact your local supplier for ordering information. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

FCC Class A

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Technical Support and Assistance

Step 1. Visit the JHC web site at www.jhctech.com.cn where you can find the latest information about the product.

Step 2. Contact your distributor, sales representative, or JHC's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:

- Product name and serial number
- Description of your peripheral attachments
- Description of your software (operating system, version,application software, etc.)
- A complete description of the problem
- The exact wording of any error messages

CONTENTS

CHAPTER 1

General Information

1.1 Introduction

KMDA-2631,equipped with Intel® Elkhart lake U series processor, with a comprehensive I/O interface, built-in 2*Mini PCIe expansion module, DC12V or 9~36V (optional) wide voltage DC power supply optional, the product adopts SGCC box design, exquisite and compact size. The main application scenario is the controller for collaborative robots.

1.2 Features

- Intel® Elkhart lake Soc CPU
- 1*DDR4 3200MHz SODIMM，Up to 32GB
- 1*mSATA，1*SATA3.0
- 3*LAN，2*USB3.1，2*USB2.0，2*(RS232/485)，4*DI+4*DO indicates isolation，1*HDMI
- 2*MiniPCIe(supports 4G, with SIM card slot, with PCIeX1 and USB2.0 signal)
- DC 12V or 9 -36V(optional) power input
- Fanless cooling design

1.3 Specifications

1.3.1 General

CPU: Intel® Elkhart lake SoC CPU: Celeron J6412 2.0-2.6GHz 4-core 4-thread

Chipset: Intel® CPU SoC MCP

Memory: 1*DDR4 3200 MHz SODIMM, up to 32GB

BIOS: AMI EFI BIOS, 128Mbit SPI flash memory

Display:1*HDMI

Store： 1*mSATA, 1*SATA3.0

USB: 2*USB3.1 (Type A)，2*USB2.0 (Type A)

Serial Ports： 2*COM: 2*RS232/485

DIO： 4*DI+4*DO, with isolation

Expansion Interface: 2*Mini-PCIe, with PCIeX1 and USB2.0 signals, can expand the PCIe signal function module, including 1*MiniPCIe, with SIM card slot, support 4G module; The other MIniPCie interface function is reserved.

1.3.2 Ethernet

Chipset: **3***RTL811H-VB, support WOL

Speed: 10M / 100M / 1000Madaptive

Interface: 2*RJ45 w/LED

1.3.3 Power Consumption

Input Voltage: Standard: 12V; DC 9~36V wide power input,， with short circuit, over voltage and over current protection

Power Consumption: 14.4W (CPU Celeron J6412 @2.00GHz，8G DDR4，128G SSD)

Power Adapter:

AC/DC power adapter · DC12V@5A ,60W

1.4 Environmental requirement

Operating temperature: 0~50℃ –HDD(–10~55℃ –SSD), with airflow

Relative humidity:10~95%@40 , non‐condensing

Storage temperature: -20 ~ 60°C

Vibration loading during operation: 1g 5~500Hz, in operating with HDD

Shock during operation: 10g peak acceleration(duration 11ms), in operating with HDD

EMC: CE, FCC Class A

1.5 Ordering Information

Model NO.	Power	Description
KMDA-2631/ S001	12V	Built-in box computer, 8*COM, 2*USB3.1+2*USB2.0, 3*LAN, 1*HDMI, 1*mSATA, 1*SATA3.0, 2*Mini PCIe with PCIeX1 and USB2.0 signals (1*MiniPCIe supports 4G, with SIM card slot, Another 1*MiniPCIe expansion port is reserved), 4*DI+4*DO.
KMDA-2631/ S001-WP	9-36V	
PA-60DC12	AC/DC power adapter, DC12V@5A ,60W	

1.6 Dimension

KMDA-2631 Dimension（Unit：mm）

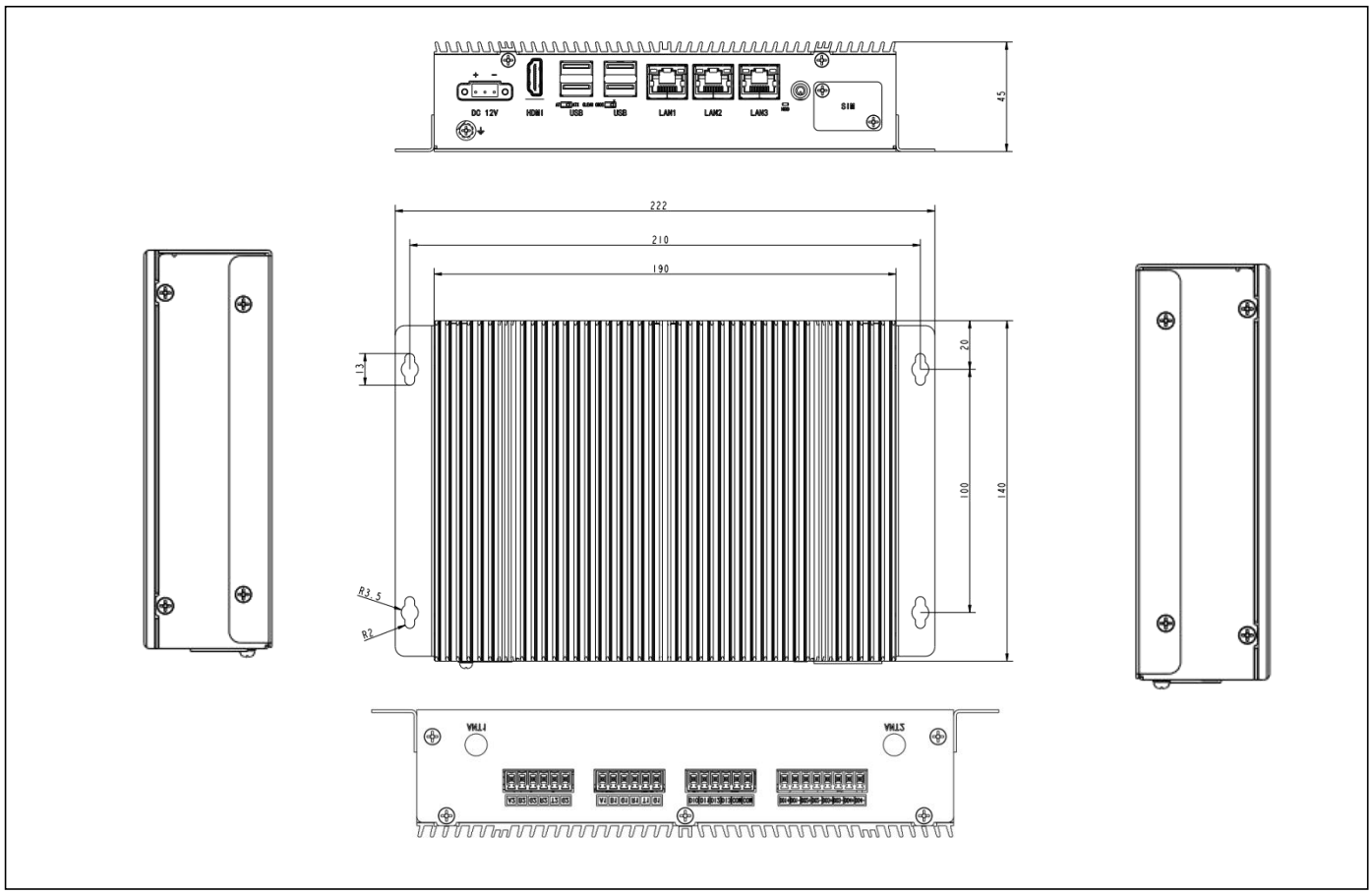


Figure 1.1

1.7 I/O Interface

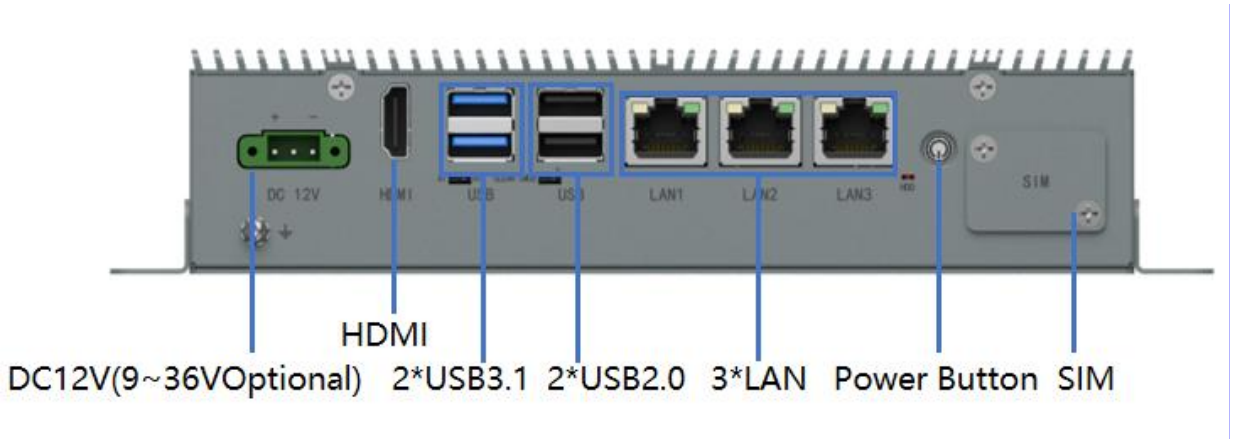


Figure 1. 2

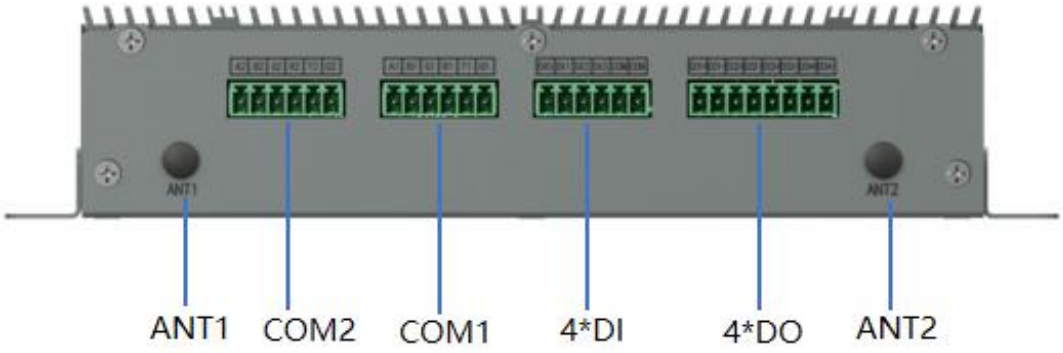


Figure 1. 3

CHAPTER 2

Hardware Installation

2.1 Introduction

The following chapters will state the panel DIP switch settings and external connectors and pin assignments of the product.

2.2 Panel DIP switch settings and jumpers

The KMDA-2631 is equipped with a simple DIP switch on the panel. This simple DIP switch can be toggled with tweezers or a card pin, which is convenient for users to set according to different configuration requirements. The following table lists the function of each DIP switch and jumpers on the panel.

DIP switch list:

Model No.	Introduction	Describe
AT/ATX	Set the power-on mode to AT or ATX	3-Pin SW
CLEAR/CMOS	Clear CMOS data and restore default settings	3-Pin SW

Jumpers list:

Model No.	Introduction	Describe
COM_SEL1	Set COM1&COM2 mode	header

2.2.1 AT/ATX Power-on mode selection switch

Figure 2.1

CLEAR Mode:Clear CMOS data ； *CLEAR Mode:Keep CMOS data

The CMOS is powered by the socket BAT battery. Clearing CMOS will permanently erase the previous system settings and set them to the original (factory settings) system settings.

When you encounter the following problems:

a) COMS data is messy and lost;

b) Forgot the super password and user password;

You can store the default values in the ROM BIOS to reconfigure your system. The steps:

(1) Turn off the computer and disconnect the power supply;

(2) Toggle the DIP switch to CLEAR mode, stay for 5~6 seconds, and then return to CMOS mode;

(3) Start the computer, press the Del key to enter the BIOS settings during startup, and reload the optimal default values;

(4) Save and exit the setting.

2.2.2 AT/ATX Power-on mode selection switch

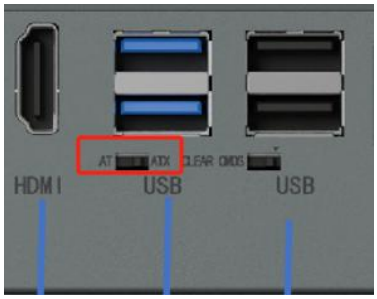


Figure 2.2

KMDA-2631 provides AT/ATX switch, users can use tweezers to toggle the DIP switch to set the machine's boot mode. When you switch it to AT mode, it means turning on the DC power and turning it on; when turning it to ATX, it means turning it on by the power switch button.

2.2.3 COM1&COM2 mode selection

COM _ SEL 1 can be used for selection of COM7 & 8. Before installation, the serial mode required by the customer should be confirmed in advance to avoid wrong selection. At the same time, the serial mode needs to be realized through the cap.

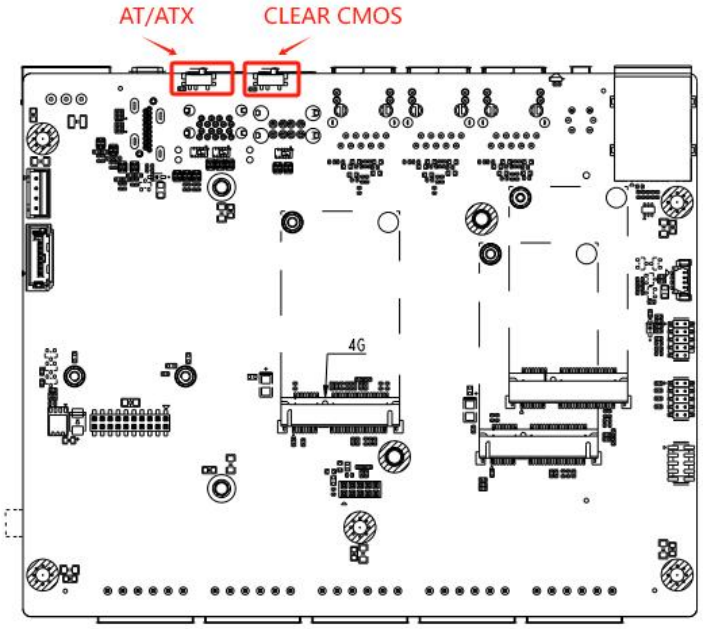


Figure 2.3

Table 2.1: COM_SEL mode selection		
	Mode	Position of jumper cap
COM7	RS232 (DEF)	3-4
	RS485	1-2
COM8	RS232 (DEF)	7-8
	RS485	5-6

2.3 I/O Introduction and Pin Assignments

2.3.1 Power Input Connector（DC-IN）

PIB-318 provides a wide pressure (9 to 36 V) input through a 3-pin terminal

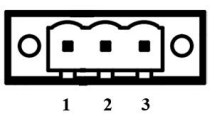


Figure 2.4 DC port

The pin assignment is described as follows：

Table 2.2: DC-IN Port Pin Assignments			
Pin	Signal	Pin	Signal

1	9~36V	2	NC
3	GND		

2.3.2 CMOS Battery

The PIB-318 provides a CMOS battery port.

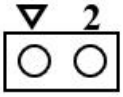


Figure2.5 The CMOS battery interface diagram

Table 2.3 CMOS battery Port Pin Assignments			
Pin	Signal	Pin	Signal
1	BAT+	2	GND

2.3.3 HDMI

PIB-318 provides 1 vertical HDMI display of the Port, with a detailed Pin assignment described below.

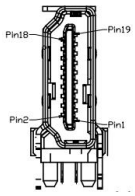


Figure2.6 HDMI Port

Table2.4 HDMI Port Pin Assignments					
Pin	Signal	Pin	Signal	Pin	Signal
1	DATA2_P	8	GND	15	SCL
2	GND	9	DATA0_N	16	SDA
3	DATA2_N	10	CLK_P	17	GND
4	DATA1_P	11	GND	18	VCC
5	GND	12	CLK_N	19	DETECT
6	DATA1_N	13	NC		
7	DATA0_P	14	NC		

2.3.4 Ethernet Port

The PIB-318 is equipped with a 3*RTL 8111H chip and supports 10/100/1000Mbps rate adaptation. This Ethernet provides the standard RJ-45 Port, the next Table for the detailed Pin assignment introduction.

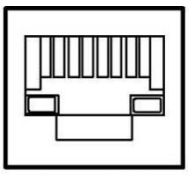


Figure2.7 Ethernet Port

Table2.5 RJ-45 Port Pin Assignments			
Pin	10/100/1000BaseT Signal	Pin	10/100/1000BaseT Signal
1	TX+(10/100), LAN_DA+(GHz)	5	LAN_DC-(GHz)
2	TX-(10/100), LAN_DA-(GHz)	6	RX-(10/100), LAN_DB-(GHz)
3	RX+(10/100), LAN_DB+(GHz)	7	LAN_DD-(GHz)
4	LAN_DC+(GHz)	8	LAN_DD-(GHz)

2.3.5 USB Port （USB3.2 Port 1/2）

PIB-318 provides 2 * USB3.2 (type A), with the ability to close USB in the BIOS. Table assigns the USB3.0 (type A) Pin with an introduction.

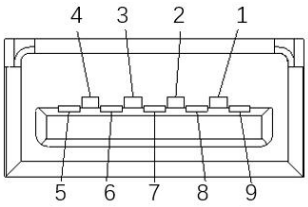


Figure2.8 USB3.0 type A Port

Table2.6 USB3.0 type A PortPin Assignments			
Pin	Signal	Pin	Signal
1	VBUS0	6	RX0+
2	D0-	7	GND
3	D0+	8	TX0-
4	GND	9	TX0+
5	RX0-	Shell	Shield

2.3.6 USB Port （USB2.0 Port 1/2）

The PIB-318 provides 2 * USB2.0 (type A), which sets up the ability to close the USB in the BIOS. Next Table assigns the USB3.0 (type A) Pin with an introduction.

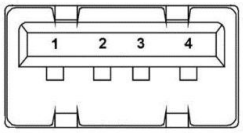


Figure2.9 USB2.0 Type A Port

Table2.7 USB2.0 type A Port Pin Assignments	
Pin	Signal
1	USB_VCC
2	USB_D-
3	USB_D+
4	USB_GND

2.3.7 COM1/2 Port

COM1 / 2 is 23.81mm-6P Phoenix terminal connector configured as RS232 or RS485 via BIOS or hop cap.

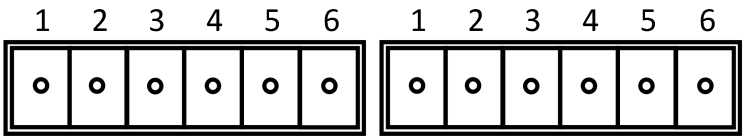


Figure2.10 COM1/2 Port

Next Table describes the detailed Pin assignments for COM1 / 2 Port .

Table2.8 COM1/2/ Port Pin assignments		
Pin	RS-232/RS-485Signal(COM1)	RS-232/RS-485Signal(COM2)
1	COM1_A1	COM2_A2
2	COM1_B1	COM2_B2
3	GND	GND
4	COM1_232_RXD	COM2_232_RXD
5	COM1_232_TXD	COM2_232_TXD
6	GND	GND

2.3.8 DIO Port

PIB-318 provides a DI of 1*8pin and two DO Port of 1*6P, and the next Table introduces a detailed Pin assignment.

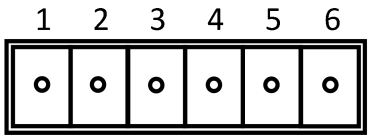


Figure2.11 DI Port

The following table provides a detailed Pin assignment introduction for the DI interface.

Table2.9 6Pin DI Port Pin Assignments

Pin	Signal	Pin	Signal
1	DIN0	2	DIN1
3	DIN2	4	DIN3
5	ECOM1	6	ECOM1

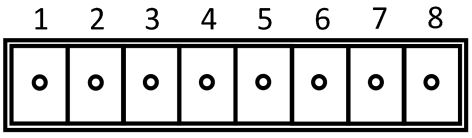


Figure2.12 DO Port

The following table provides a detailed introduction to the Pin assignments for the DO interface.

Table2.10 1*8Pin DI Port Pin Assignments			
Pin	Signal	Pin	Signal
1	DO1+	5	DO1-
2	DO2+	6	DO2-
3	DO3+	7	DO3-
4	DO4+	8	DO4-

2.3.9 SM Bus

PIB-318 provides a SM Bus Port of 4 Pin, under Table for a detailed Pin assignment introduction.

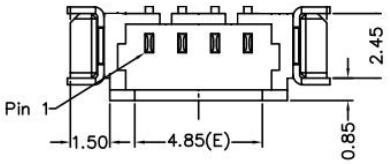


Figure 2.13 SM Bus Port

Table2.11 SMB Port Pin Assignments			
Pin	Signal	Pin	Signal
1	GND	2	DAT
3	CLK	4	+V3.3

2.3.10 SATA Port 1

PIB-318 provides a SATA Port of 1 * 7pin, and the following table gives a detailed introduction to the pin assignment.

Figure 2.14 SATA Port

Table2.12 7Pin SATA POwer Port Pin Assignments			
Pin	Signal	Pin	Signal
1	GND	5	RX-
2	TX+	6	RX+
3	TX-	7	GND
4	GND		

2.3.11 SATA Port (wafer)

PIB-318 provides a SATA Pin of 1*4pin internally, under Table for a detailed Pin assignment introduction.

Figure 2.15 SATA Power Port

Table2.13 4Pin SATA Port Pin Assignments			
Pin	Signal	Pin	Signal
1	5V	3	GND
2	GND	4	12V

2.3.12 Mini-PCIe Port

PIB-318 provides three Mini-PCIe Port, one 4G, one mSATA, and one reservation. The following table is a detailed introduction of Pin assignmen.

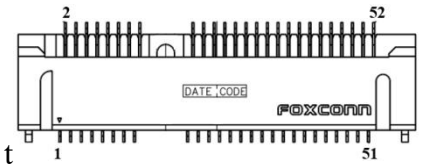


Figure2.16 Mini-PCIe Port

Table2.14 Mini-PCIe Port Pin Assignments			
Pin	Signal	Pin	Signal
1	PCIE_WAKE_N	2	+V3.3_MINICARD2
3	NC	4	GND
5	NC	6	+V1.5
7	+V3.3_MINICARD2	8	+VUIM_PWR
9	GND	10	UIM_DATA
11	CLK_MIO1_PCIE-	12	UIM_CLK
13	CLK_MIO1_PCIE+	14	UIM_RESET
15	GND	16	+VUIM_VPP
17	NC	18	GND
19	NC	20	WIFI2_DISABLE#

21	GND	22	PLTRST#
23	PCIE_MINI_RX2-	24	+V3.3_MINICARD2
25	PCIE_MINI_RX2+	26	GND
27	GND	28	+V1.5
29	GND	30	SMB_SCL_RSM
31	PCIE_MINI_TX2-	32	SMB_SDA_RSM
33	PCIE_MINI_TX2+	34	GND
35	GND	36	USB_N5
37	GND	38	USB_N5
39	+V3.3_MINICARD2	40	GND
41	+V3.3_MINICARD2	42	NC
43	GND	44	NC
45	NC	46	NC
47	NC	48	+V1.5
49	NC	50	GND
51	NC	52	+V3.3_MINICARD2

2.3.13 CPU FAN

The AXM-I719 on the motherboard offers 1 * 4pin wafer SMT90 1.25mm pitch.

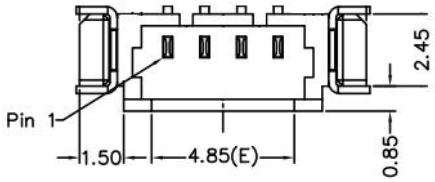


Figure2.17 CPU FAN Port

Table2.15 CPU FAN Port Pin Assignments			
Pin	Signal	Pin	Signal
1	GND	2	VCC
3	Control	4	Tachometer

2.3.14 Expansion I/O MXM 3.1 Goldfinger(281-Pin)

Goldfinger on the motherboard is as follows, the actual design of the hardware can be adjusted according to the situation. The need to increase the handshake signal can be achieved by reducing the serial port signal.

Table2.16 Goldfinger Assignments			
Pin	Signal	Pin	Signal
E1	MXM_DC_IN 12V	E2	MXM_DC_IN 12V
E3	GND	E4	GND

1	+VBAT	2	PLTRST_N
3	+VCCPAZIO_3P3_1P8	4	PCIE_WAKE-
5	AC_RST-	6	IO_BOARD_PWROK
7	I2S_MCLK	8	IO_BOARD_PWROK
9	AC_SYNC	10	/
11	AC_SDIN0	12	GND
13	AC_SDOUT	14	SLP_S3-
15	AC_BITCLK	16	SLP_S4_N
17	GND	18	RTCRST#
19	24M_SIO_PCICLK	20	SATA_LED-
21	ESPI_ IO0（LAD0）	22	GND
23	ESPI_IO1（LAD1）	24	GND
25	ESPI_IO2（LAD2）	26	SATAPCIE_2
27	ESPI_ IO3（LAD3）	28	SATAPCIE_3
29	ESPI_RST#	30	SMLOALERT#
31	ESPI_ CS0#(LFRAME#)	32	PCH_SMB_CK
33	ESPI_CS1#(SERIRQ#)	34	PCH_SMB_DA
35	ESPI_ ALERT#(PIRQA#)	36	GND
37	GND	38	CPU PCIE3_TXN
39	CPU PCIE3_RXN	40	CPU PCIE3_TXP
41	CPU PCIE3_RXP	42	CPU PCIE2_TXN
43	CPU PCIE2_RXN	44	CPU PCIE2_TXP
45	CPU PCIE2_RXP	46	GND
47	GND	48	CLK_PE_PORT2_N
49	CLK_PE_PORT1_N	50	CLK_PE_PORT2_P
51	CLK_PE_PORT1_P	52	GND
53	GND	54	CPU PCIE1_TXN
55	CPU PCIE1_RXN	56	CPU PCIE1_TXP
57	CPU PCIE1_RXP	58	GND
59	GND	60	CPU PCIE0_TXN
61	CPU PCIE0_RXN	62	CPU PCIE0_TXP
63	CPU PCIE0_RXP	64	GND
65	GND	66	PCIE12_TXN(SATA3_TX_N1)
67	PCIE12_RXN(SATA3_RX_N1)	68	PCIE12_TXP(SATA3_TX_P1
69	PCIE12_RXP(SATA3_RX_P1)	70	GND
71	GND	72	PCIE11_TXN(SATA3_TX_N0)
73	PCIE11_RXN(SATA3_RX_N0)	74	PCIE11_TXP(SATA3_TX_P0
75	PCIE11_RXP(SATA3_RX_P0)	76	GND
77	GND	78	SIO UART6_DN
79	SIO UART5_DN	80	SIO UART6_PN
81	SIO UART5_PN	82	GND
83	GND	84	PCIE10_TXN
85	PCIE10_RXN	86	PCIE10_TXP
87	PCIE10_RXP	88	GND

89	GND	90	PCIE9_TXN
91	PCIE9_RXN	92	PCIE9_TXP
93	PCIE9_RXP	94	GND
95	GND	96	PCIE8_TXN
97	PCIE8_RXN	98	PCIE8_TXP
99	PCIE8_RXP	100	GND
101	GND	102	PCIE7_TXN
103	PCIE7_RXN	104	PCIE7_TXP
105	PCIE7_RXP	106	GND
107	GND	108	PCIE6_TXN
109	PCIE6_RXN	110	PCIE6_TXP
111	PCIE6_RXP	112	GND
113	GND	114	PCIE5_TXN
115	PCIE5_RXN	116	PCIE5_TXP
117	PCIE5_RXP	118	GND
119	GND	120	PCIE4_TXN(USB3_P4_TX_DN
121	PCIE4_RXN(USB3_P4_RX_DN)	122	PCIE4_TXP(USB3_P4_TX_DP
123	PCIE4_RXP(USB3_P4_RX_DP)	124	GND
125	GND	126	SIO UART3_DN
127	SIO UART4_DN	128	SIO UART3_PN
129	SIO UART4_PN	130	/
131	/	132	/
133	GND	134	GND
135	PCIE3_RXN(USB3_P3_RX_DN)	136	PCIE3_TXN(USB3_P3_TX_DN
137	PCIE3_RXP(USB3_P3_RX_DP)	138	PCIE3_TXP(USB3_P3_TX_DP
139	GND	140	GND
141	PCIE2_RXN(USB3_P2_RX_DN)	142	PCIE2_TXN(USB3_P2_TX_DN
143	PCIE2_RXP(USB3_P2_RX_DP)	144	PCIE2_TXP(USB3_P2_TX_DP
145	GND	146	GND
147	PCIE1_RXN(USB3_P1_RX_DN)	148	PCIE1_TXN(USB3_P1_TX_DN
149	PCIE1_RXP(USB3_P1_RX_DP	150	PCIE1_TXP(USB3_P1_TX_DP
151	GND	152	GND
153	CLK_PE_PORT0_N	154	GSPI0_CLK
155	CLK_PE_PORT0_P	156	GSPI0_MISO
157	GND	158	GSPI0_MOSI
159	SMLINK0_CLK	160	GSPI0_CS0#
161	SMLINK0_DATA	162	I2C1_SCL(NON UART3_DN)
163	LAN_WAKE#	164	I2C1_SDA((NON UART3_DP)
165	LANPHYPC	166	GND
167	USB_OC0	168	CLK_PE_PORT4_N
169	USB_OC1	170	CLK_PE_PORT4_P
171	USB_OC2	172	GND
173	GND	174	USB2_N1
175	CLK_PE_PORT3_N	176	USB2_P1

177	CLK_PE_PORT3_P	178	GND
179	GND	180	USB2_N3
181	CLK_PE_PORT5_N	182	USB2_P3
183	CLK_PE_PORT5_P	184	GND
185	GND	186	USB2_N5
187	USB2_N2	188	USB2_P5
189	USB2_P2	190	GND
191	GND	192	USB2_N7
193	USB2_N4	294	USB2_P7
195	USB2_P4	196	GND
197	GND	198	USB2_N9
199	USB2_N6	200	USB2_P9
201	USB2_P6	202	GND
203	GND	204	USB2_N10
205	USB2_N8	206	USB2_P10
207	USB2_P8	208	GND
209	GND	210	GND
211	GND	212	GND
213	GND	214	GND
215	GND	216	GND
217	GND	218	GND
219	GND	220	GND
221	GND	222	GND
223	GND	224	GND
225	GND	226	GND
227	GND	228	GND
229	GPP_B_14_SPKR	230	DCD2#
231	DCD1#	232	RI2#
233	RI1#	234	CTS2#
235	CTS1#	236	DTR2#
237	DTR1#/JP4	238	RTS2#
239	RTS1#/JP2	240	DSR2#
241	DSR1#	242	SOUT2
243	SOUT1/JP3	244	SIN2
245	SIN1	246	GND
247	DDPB_CPU_CLK	248	CPU_DDI2_TN0
249	DDPB_CPU_DATA	250	CPU_DDI2_TP0
251	GND	252	GND
253	CPU_DDI1_TN0	254	CPU_DDI2_TN1
255	CPU_DDI1_TP0	256	CPU_DDI2_TP1
257	GND	258	GND
259	CPU_DDI1_TN1	260	CPU_DDI2_TN2
261	CPU_DDI1_TP1	262	CPU_DDI2_TP2
263	GND	264	GND

265	CPU_DDI1_TN2	266	CPU_DDI2_TN3
267	CPU_DDI1_TP2	268	CPU_DDI2_TP3
269	GND	270	GND
271	CPU_DDI1_TN3	272	CPU_DDI2_AUXN
273	CPU_DDI1_TP3	274	CPU_DDI2_AUXP
275	GND	276	CPU_DDI2_HDP_B
277	CPU_DDI1_AUXN	278	DDPC_CPU_CLK
279	CPU_DDI1_AUXP	294	DDPC_CPU_DATA
281	CPU_DDI1_HDP_B		

2.4 Installation

This section describes the DIMM, mSATA module, Mini PCIe, and system installation methods.

2.4.1 Internal memory installation

Step 1: Remove the phillips screws on the bottom cover of the machine (as shown in the red area in the picture)

Figure 2.18

Step 2: As shown in Figure 2.19, remove the phillips screws on the back of the machine (as shown in the red area in the figure);

Figure 2.19

Step 3: Open the front and back of the machine, you can see the following assembly structure, the front panel and the board are combined, as shown in Figure 2.20, the back cover is combined with the heat dissipation profile;

Figure 2.20

Step 4: Open the front panel and motherboard of the machine, and you can see the installation structure of the board, which is a structure of motherboard + carrier board

Figure 2.21

Step 5: As shown in Figure 2.22, the mainboard is the MXM-I719 module of the NOde series. Open the latch in the red area to replace another type of memory module.

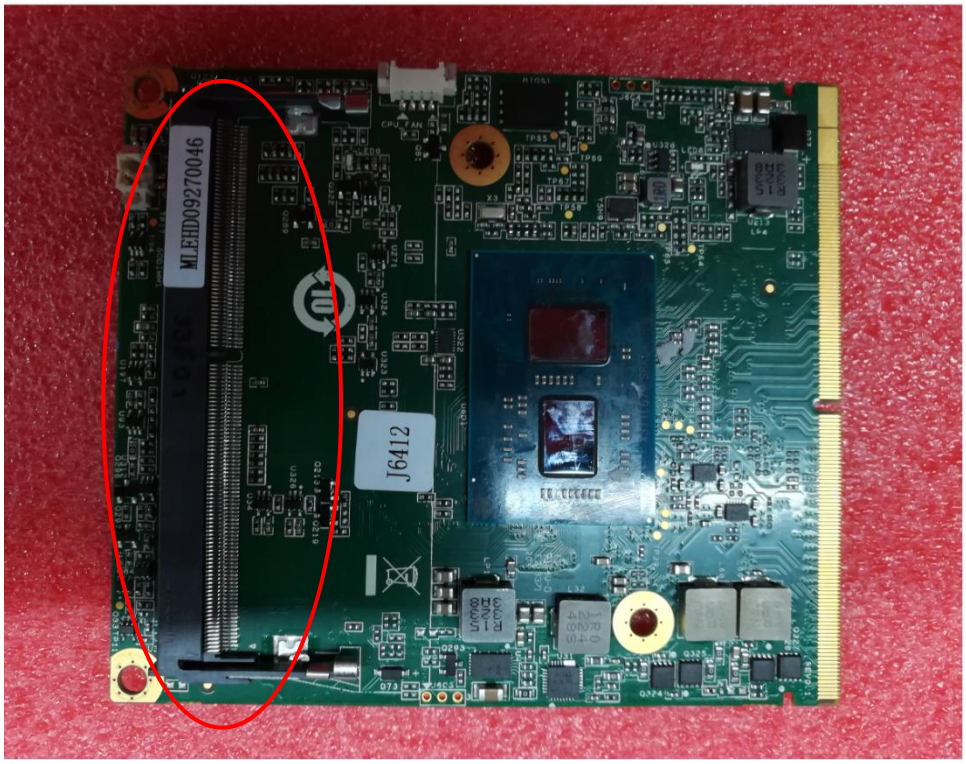


Figure 2.22

Step 6: Complete the installation of the product according to the reverse dismantling steps.

2.4.2 mSATA installation

Step 1: same as "2.4.1 Steps 1, 2, 3, 4";

Step 2: Install the mSATA module as shown in Figure 2.23.

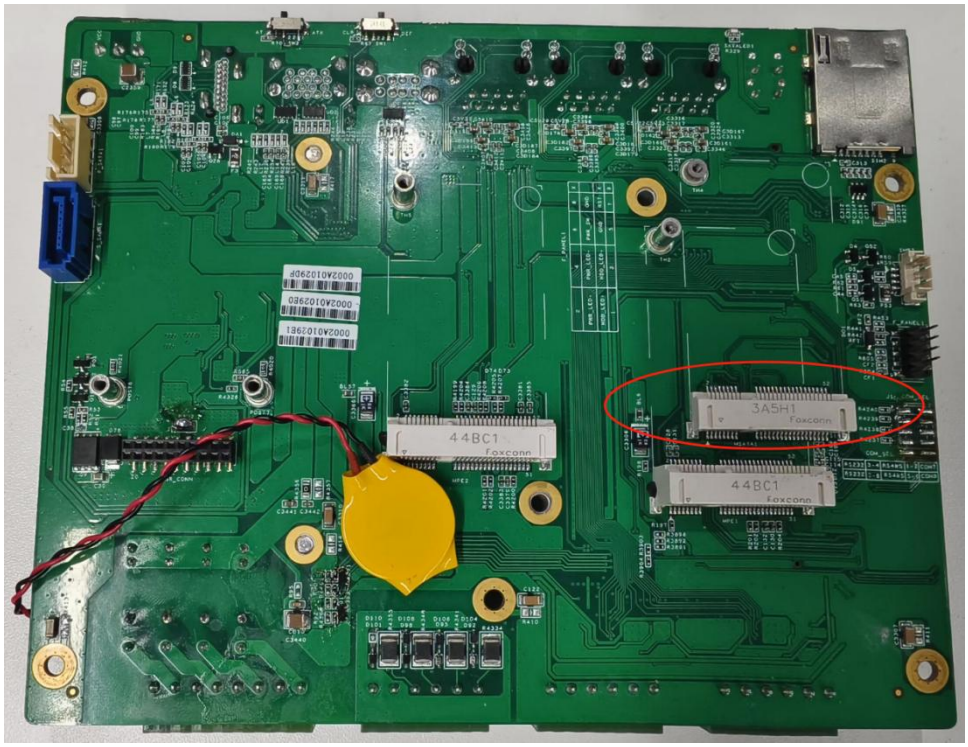


Figure 2.23

Step 3: Attach the mSATA module to the bracket with a screw.

Step 4: Complete the installation of the product by following the reverse dismantling steps.

2.4.2 miniPCIe installation

Step 1: same as "2.4.1 Steps 1, 2, 3, 4";

Step 2: As shown in Figure 2.4.10, install 4G+WIFI module here, and reserve another miniPCIe interface function. Both miniPCIe interfaces support PCIeX1 and USB2.0 signals.

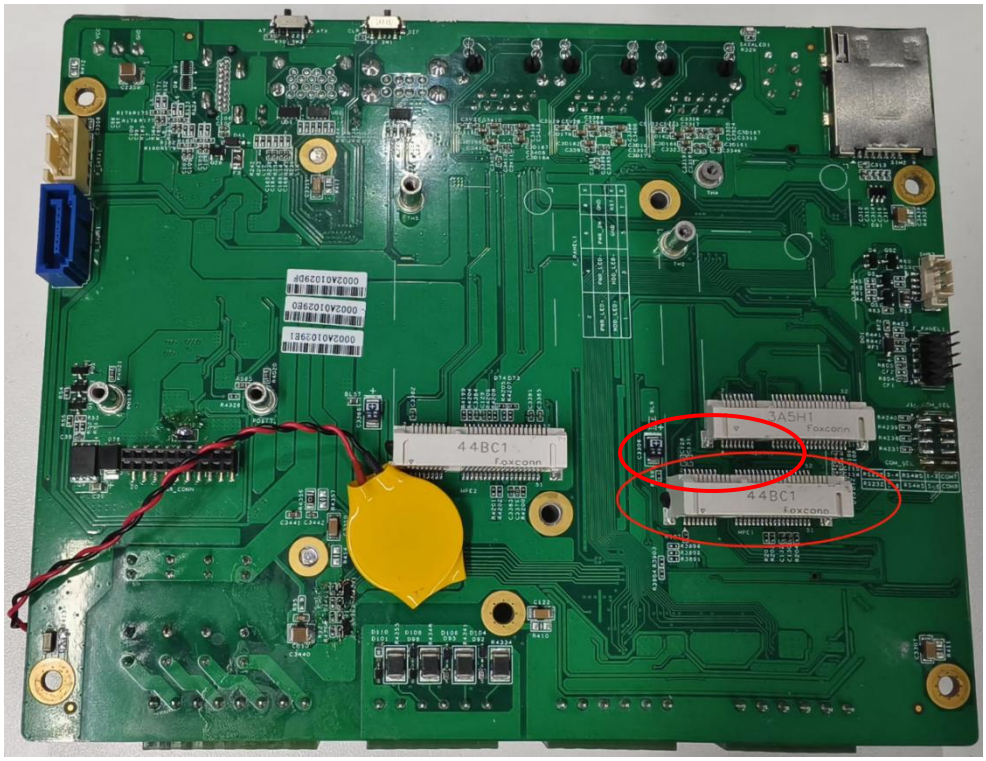


Figure 2.24

Step 3: Attach the miniPCIe module to the bracket with a screw.

Step 4: Complete the installation of the product by following the reverse dismantling steps.

CHAPTER 3

BIOS Setup

3.1 BIOS Description

BIOS is the communication bridge between hardware and software. How to correctly set the BIOS parameters is crucial for the system to work stably and whether the system works at its best.

This chapter describes how to change the system settings through the BIOS settings.

Note: For the purpose of better product maintenance, the manufacture reserves the right to change the BIOS items presented in this manual. The BIOS setup screens shown in this chapter are for reference only and may differ from the actual BIOS.

You need to make SETUP settings as follows:

1. An error message appears on the screen during the system self-test and asks for the SETUP setting.
2. You want to change the factory default settings based on customer characteristics.

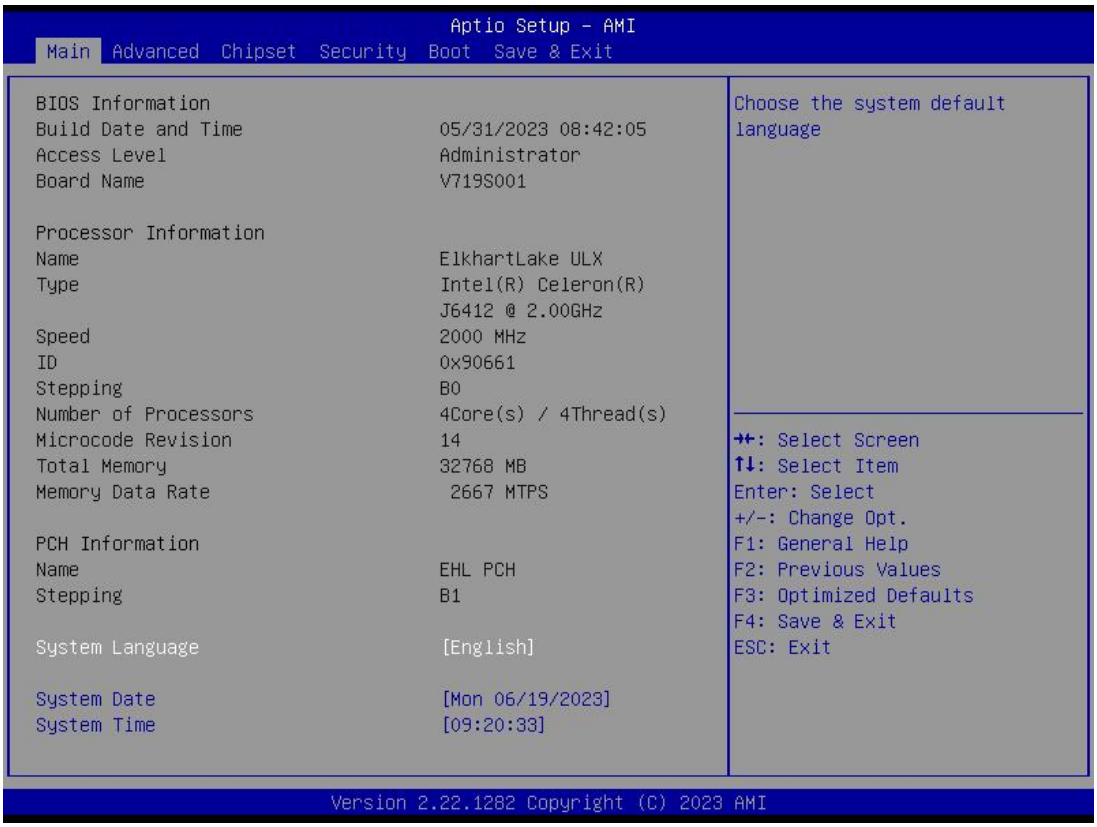
(But in general, customers are not recommended to set it up. In most cases, using the default value is already the best setting.)

The BIOS Setup Utility enables you to configure:

- Hard drives, diskette drives and peripherals
- Video display type and display options
- Password protection from unauthorized use
- Power Management features

3.1.1 Entering the Setup Utility

When you power on the system, BIOS enters the Power-On Self-Test (POST) routines. POST is a series of built-in diagnostics performed by the BIOS. After the POST routines are completed, Press the "**DEL**" key to enter BIOS Setup Utility.



3.2 BIOS parameter settings

When you start the Setup Utility, the main menu appears. The main menu of the Setup Utility displays a list of the options that are available. A highlight indicates which option is currently selected. Use the cursor arrow keys to move the highlight to other options. When an option is highlighted, execute the option by pressing <Enter>.

Some options lead to pop-up dialog boxes that prompt you to verify that you wish to execute that option. Other options lead to dialog boxes that prompt you for information.

Some options (marked with a triangle ▶) lead to submenus that enable you to change the values for the option. Use the cursor arrow keys to scroll through the items in the submenu.

In this manual, default values are enclosed in parenthesis. Submenu items are denoted by a triangle ▶.

The default BIOS setting for this motherboard apply for most conditions with optimum performance. We do not suggest users change the default values in the BIOS setup and take no responsibility to any damage caused by changing the BIOS settings.

3.2.1 BIOS Navigation Keys

Enter the SETUP settings interface, The BIOS navigation keys are listed below:

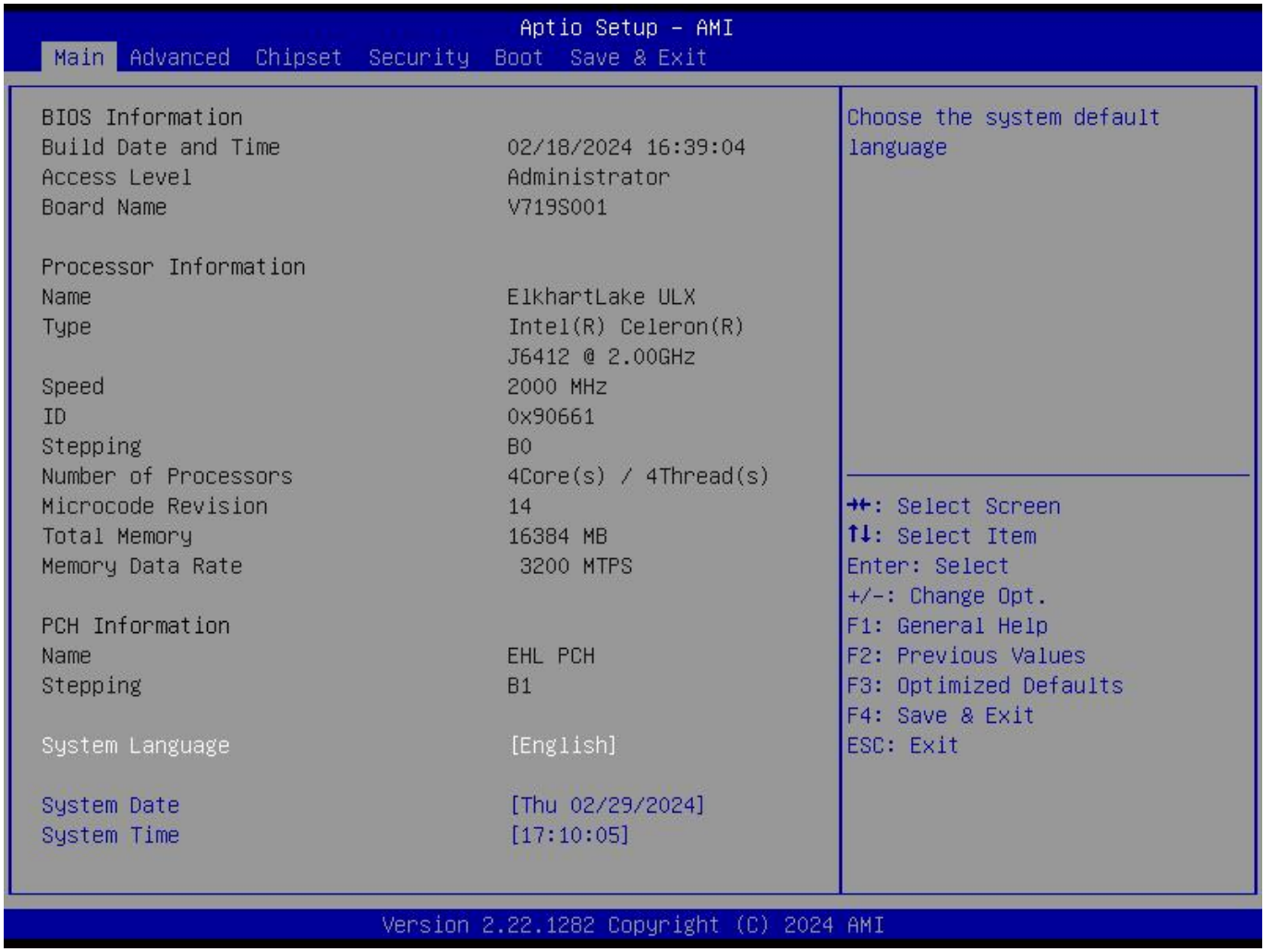
Table 3.1: The BIOS navigation keys

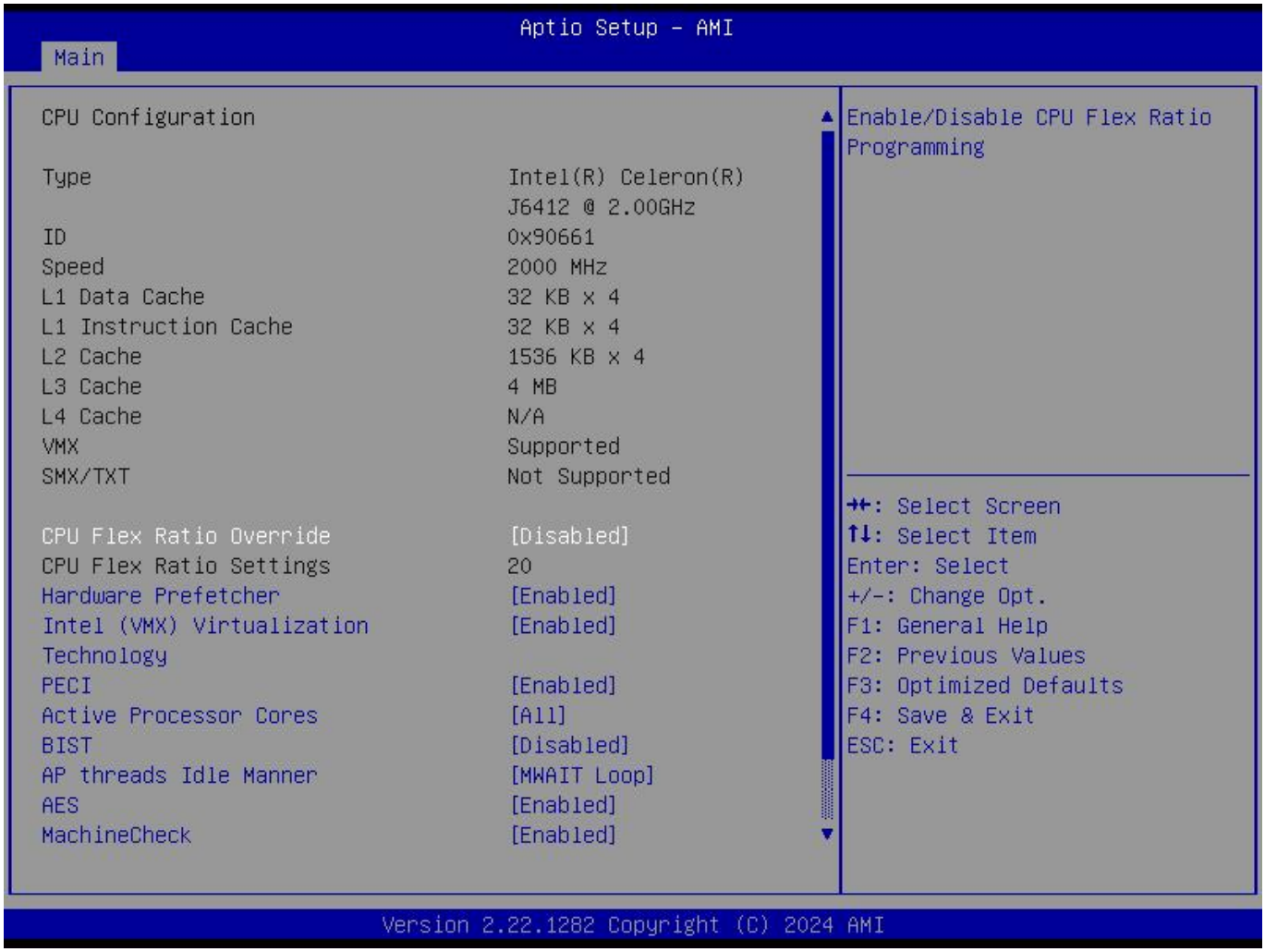
KEY	FUNCTION
ESC	Exit the current menu
↑↓→←	Scrolls through the items on a menu
+/-	Change Opt.
Enter	Select
F1	General Help
F2	Previous Values
F3	Optimized Defaults
F4	Save & Exit

3.2.2 Main Menu

When you enter the BIOS Setup program, the main menu appears, giving you an overview of the basic system information. Select an item and press <Enter> to display the submenu. Press <Esc> to back to the main menu.

The BIOS setup program provides a help screen. You can call up this help screen from any menu by simply pressing the <F1> key. This help screen lists the corresponding keys and possible selections. Press <Esc> to exit the help screen.


Aptio Setup - AMI
Main Advanced Chipset Security Boot Save & Exit
BIOS Information
Build Date and Time 02/18/2024 16:39:04
Access Level Administrator
Board Name V719S001
Processor Information
Name ElkhartLake ULX
Type Intel(R) Celeron(R)
J6412 @ 2.00GHz
Speed 2000 MHz
ID 0x90661
Stepping B0
Number of Processors 4Core(s) / 4Thread(s)
Microcode Revision 14
Total Memory 16384 MB
Memory Data Rate 3200 MTPS
PCH Information
Name EHL PCH
Stepping B1
System Language [English]
System Date [Thu 02/29/2024]
System Time [17:10:05]
Choose the system default language
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1282 Copyright (C) 2024 AMI



BIOS Vendor (American Megatrends)

This item shows the information of the BIOS vendor.

Core Version (5.13)

This item shows the information of the Core Version.

Project Version (V909S 0.01 X64)

This item shows the information of the motherboard Version.

Build Date and Time

This item shows the information of the BIOS build date and time

Processor Information

This item shows the basic information about the currently used processor, including name, type, speed.

IGFX VBIOS Version

This item shows the Current VBIOS version of the CPU integrated graphics.

Total Memory

This item shows the total memory size of the current motherboard.

Memory Frequency

This item shows the current memory operating frequency.

PCH Information

This item shows the basic information about PCH, including name, PCH SKU, etc.

System Language

Set the language interface of the BIOS.

System Date

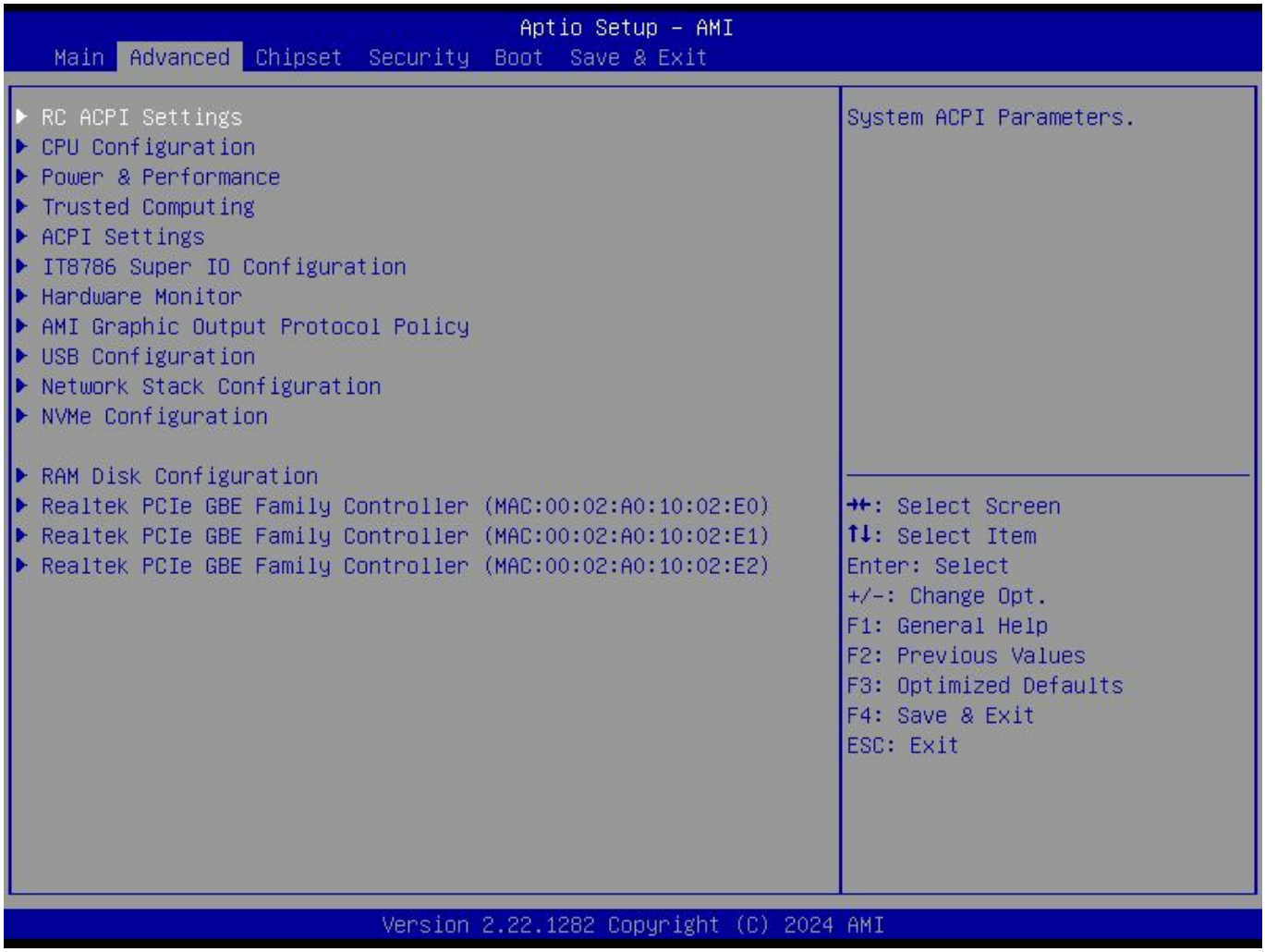
Set the date. The format of the date is <week><month><day><year>.

System Time

Set the time. The format of the time is <hour><minute><second>.

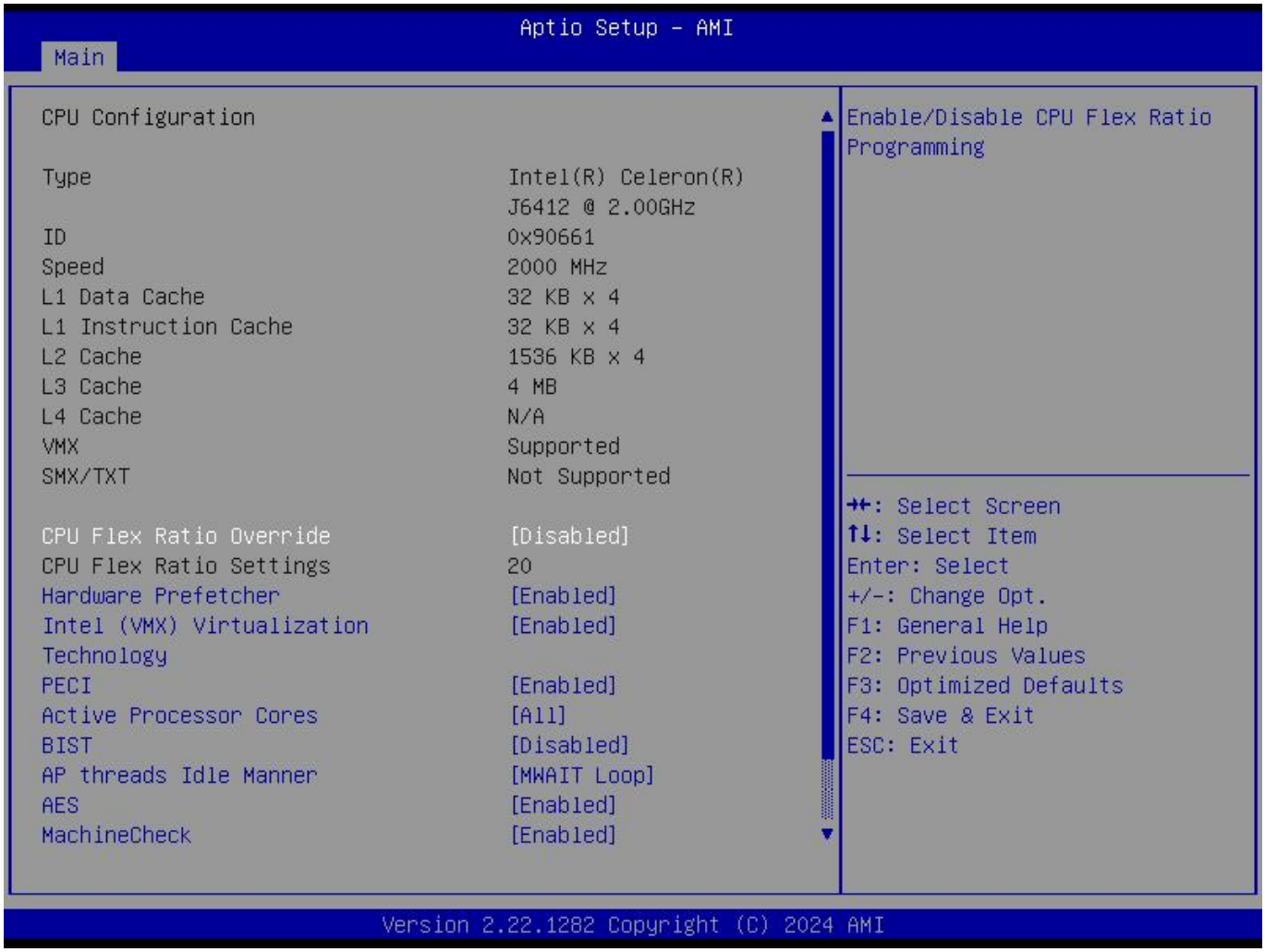
3.2.3 Advanced Menu

This page sets up more advanced information about your system. Handle this page with caution. Any changes can affect the operation of your computer.



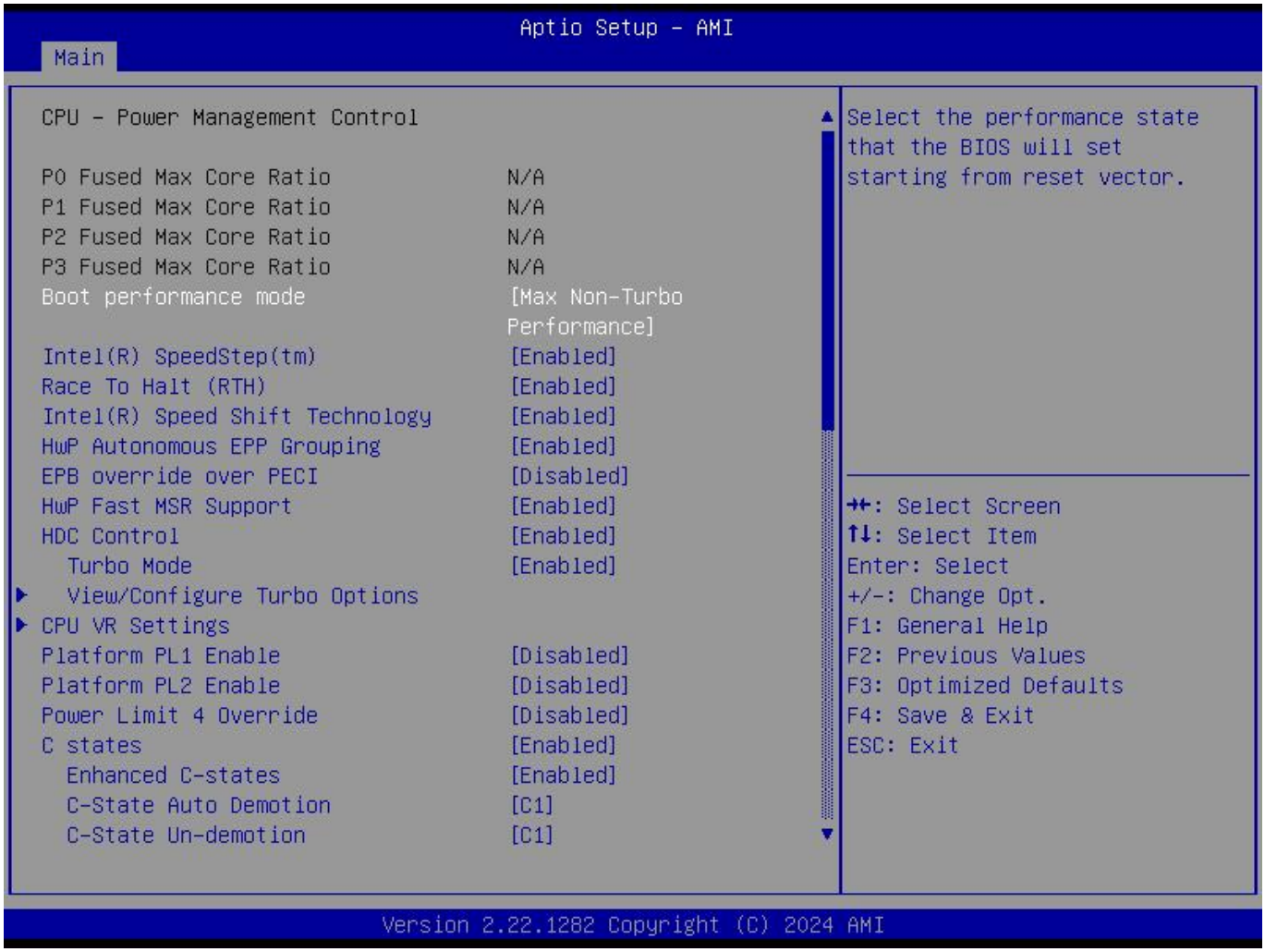
▶CPU Configuration

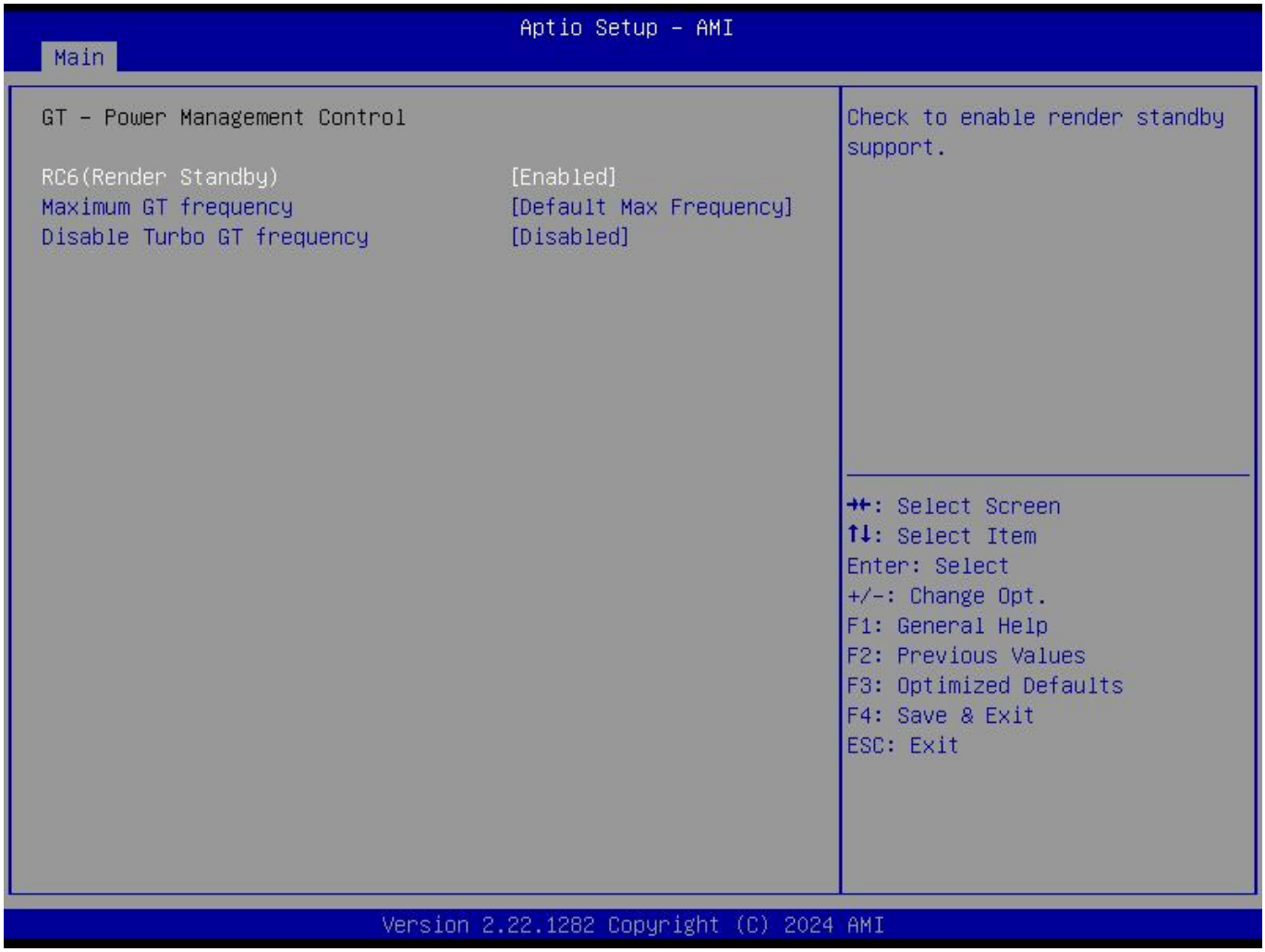
The configuration of the central processor, enter this sub-menu, there will be detailed details of the CPU, as well as various settings of the CPU.



▶Power & Performance

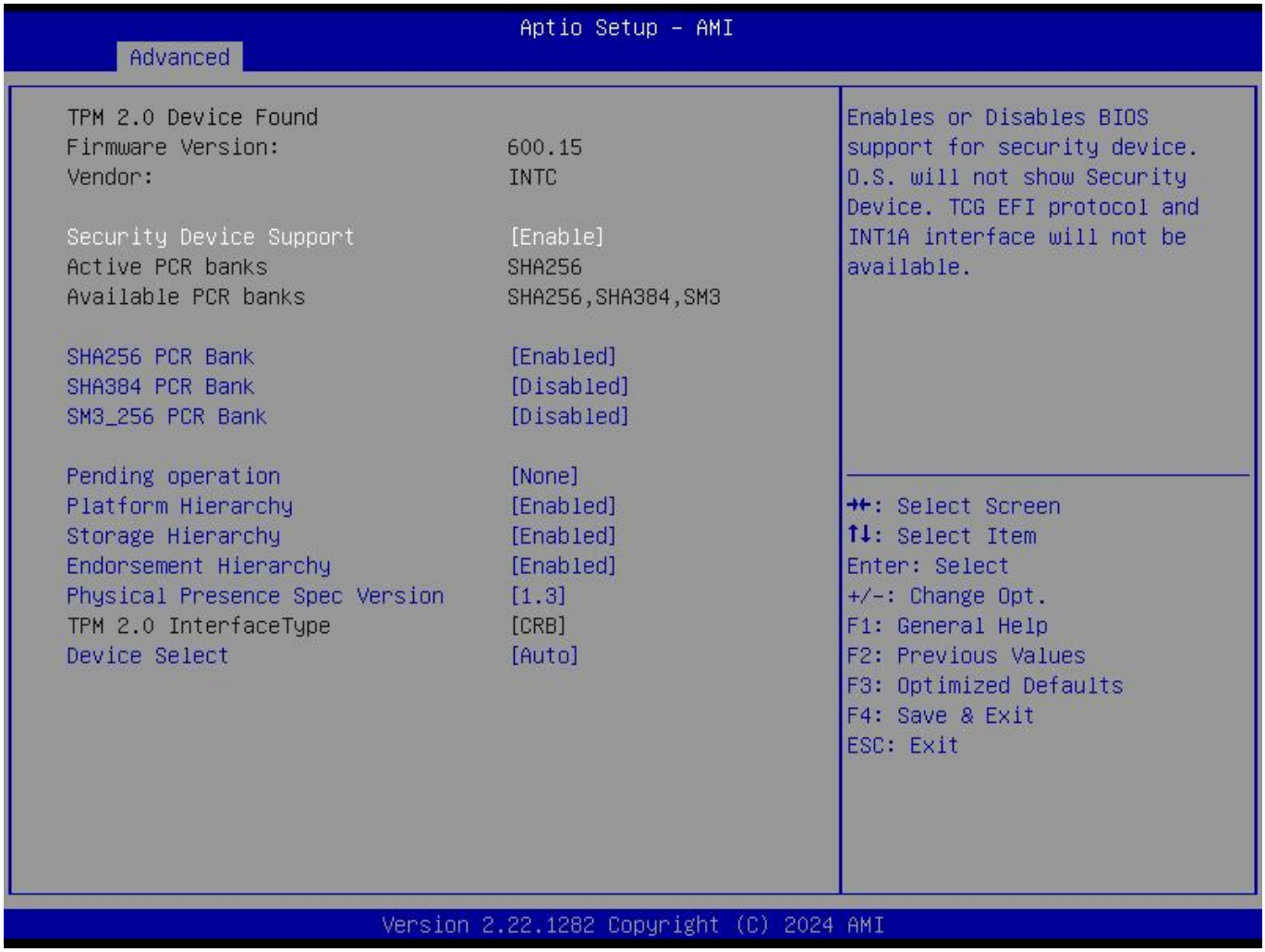
This item in the menu shows how to set the Power Management Control of CPU and GT.


Aptio Setup - AMI
Main
CPU - Power Management Control
P0 Fused Max Core Ratio N/A
P1 Fused Max Core Ratio N/A
P2 Fused Max Core Ratio N/A
P3 Fused Max Core Ratio N/A
Boot performance mode [Max Non-Turbo Performance]
Intel(R) SpeedStep(tm) [Enabled]
Race To Halt (RTH) [Enabled]
Intel(R) Speed Shift Technology [Enabled]
HwP Autonomous EPP Grouping [Enabled]
EPB override over PECI [Disabled]
HwP Fast MSR Support [Enabled]
HDC Control [Enabled]
Turbo Mode [Enabled]
View/Configure Turbo Options
CPU VR Settings
Platform PL1 Enable [Disabled]
Platform PL2 Enable [Disabled]
Power Limit 4 Override [Disabled]
C states [Enabled]
Enhanced C-states [Enabled]
C-State Auto Demotion [C1]
C-State Un-demotion [C1]
Select the performance state that the BIOS will set starting from reset vector.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1282 Copyright (C) 2024 AMI



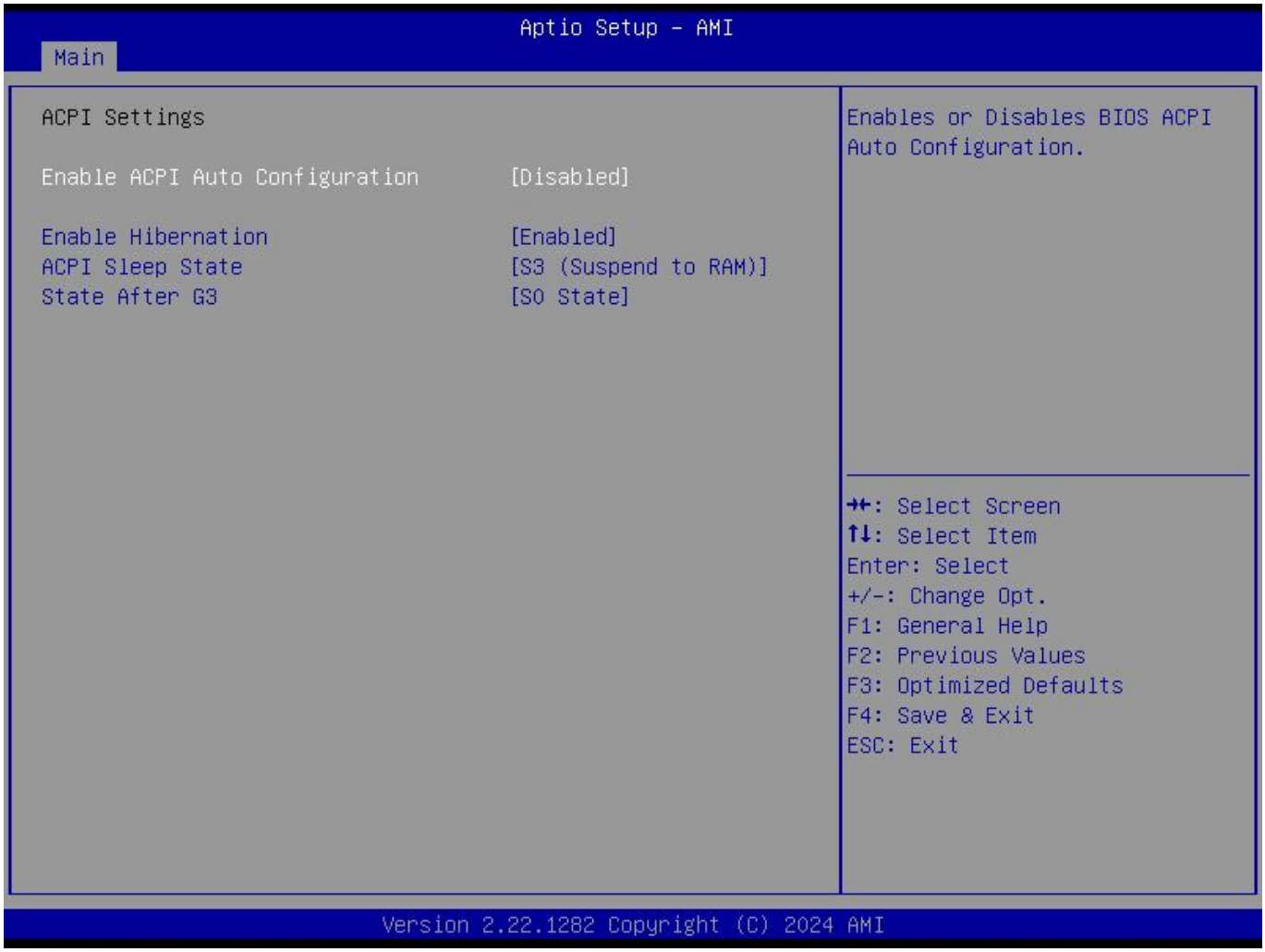
▶Trusted Computing

Trusted computing, enter this sub-menu, there will be the setting of the encryption security module (the motherboard will install the encryption module hardware will take effect)



▶ACPI Settings

Advanced configuration and power management interface settings, enter this submenu, there will be ACPI related settings.



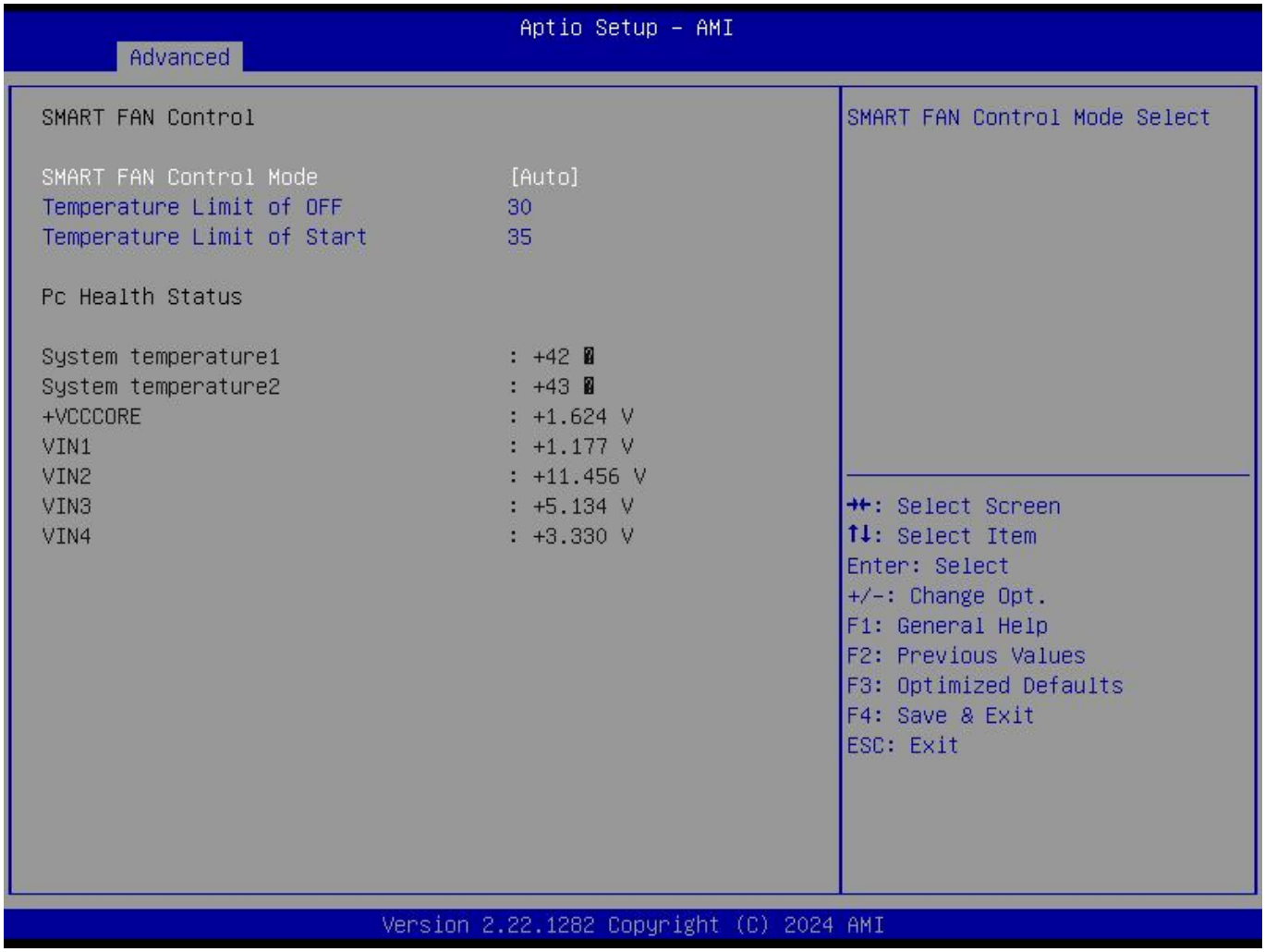
ACPI Sleep State (S3 (Suspend to RAM))

This item allows user to enter the ACPI S3 (Suspend to RAM) Sleep State (default).

Press <Esc> to return to the Advanced Menu page.

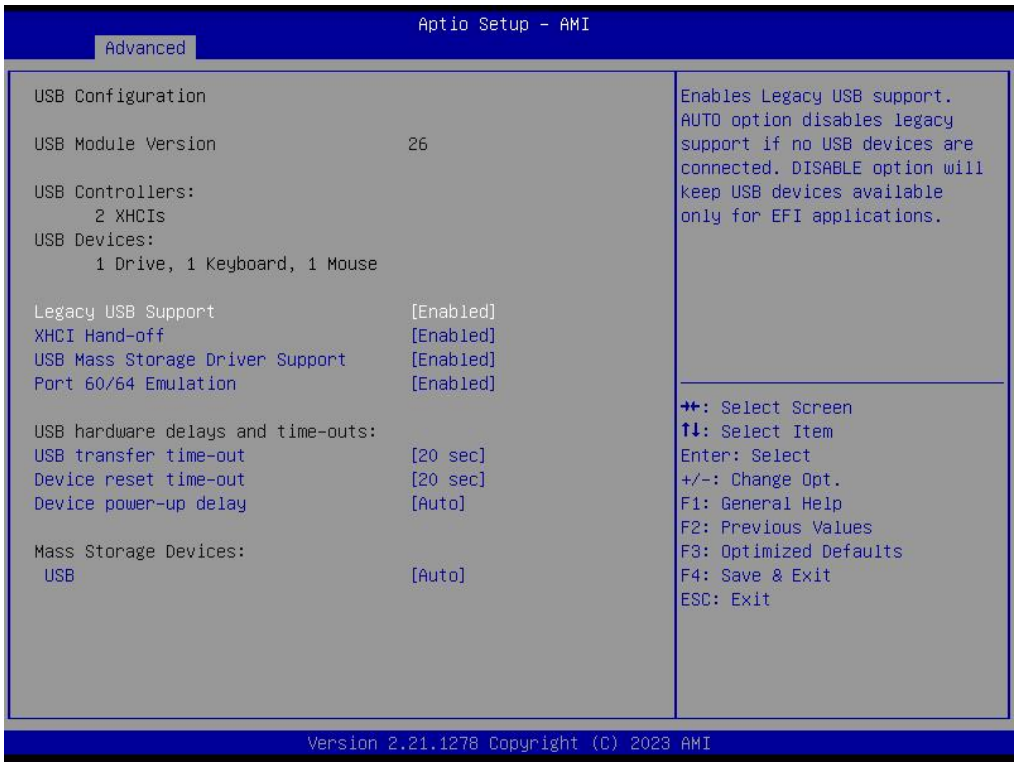
▶Hardware Monitor

Hardware monitoring, enter this sub-menu, there will be CPU temperature, System temperature, status display of each common working voltage.



▶USB Configuration

USB configuration, enter this sub-menu, there will be USB-related detailed settings.



Legacy USB Support

This item is used to set the USB interface support. If you need to support USB devices under DOS, such as U disk, USB keyboard, etc., set this item to [Enabled]. Otherwise, select [Disabled].

USB Mass Storage Driver Support

USB mass storage device support switch.

USB Transfer time-out

This item Sets the timeout period for control, batch, and interrupt transmission. The default is 20 seconds.

Device reset time-out

This item sets boot command timeout of the large capacity USB disk. The default is 20 seconds.

Device power-up delay

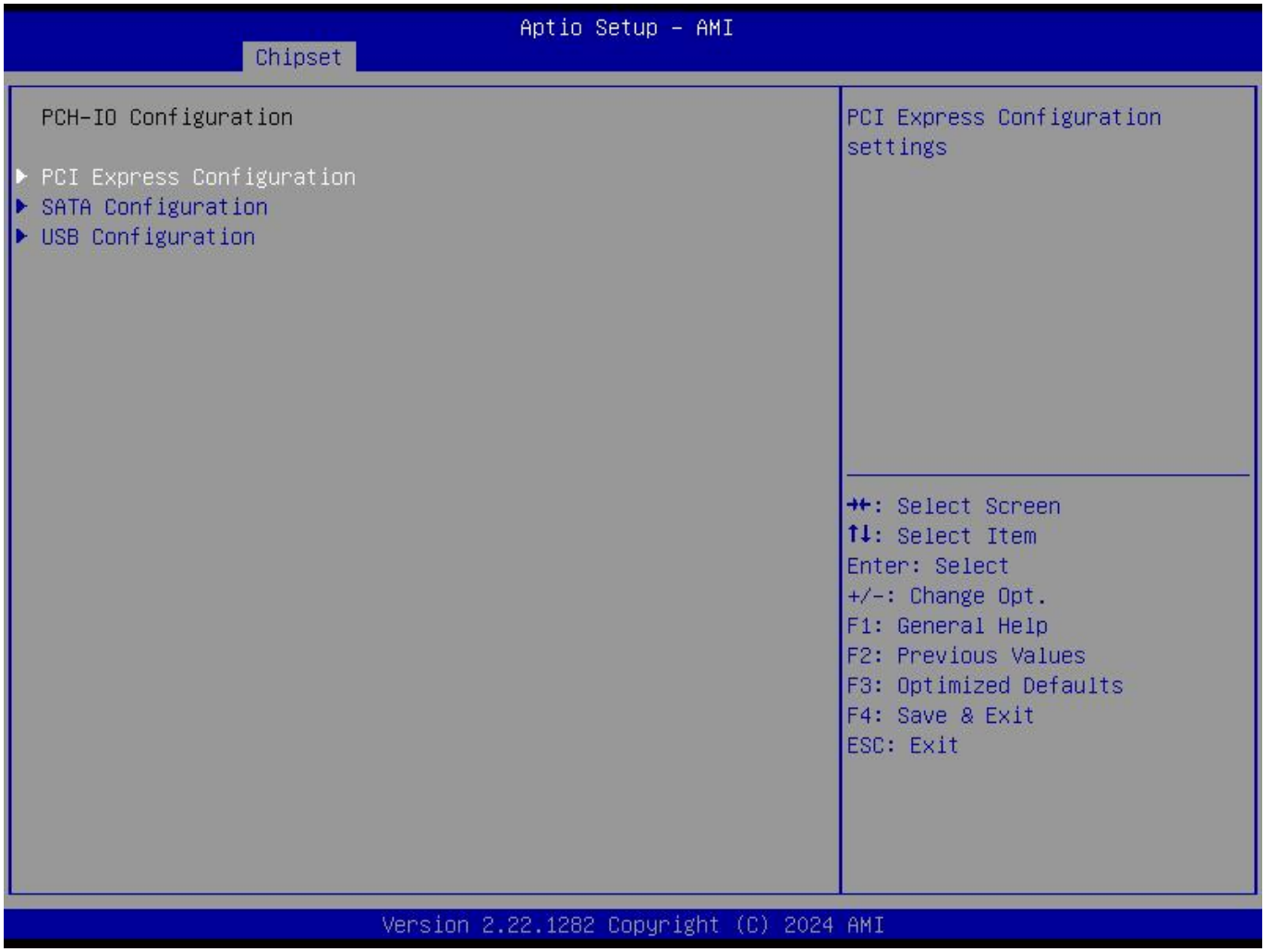
This item sets boot command delay of the large capacity USB disk. The default is Auto.

3.2.4 Chipset Menu

The chipset menu items allow you to change the settings for the North Bridge chipset, South Bridge chipset and other system.

PCH-IO Configuration (South Bridge Configuration)

▶PCI Express Configuration


Aptio Setup - AMI
Chipset
PCH-IO Configuration
PCI Express Configuration
SATA Configuration
USB Configuration
PCI Express Configuration settings
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
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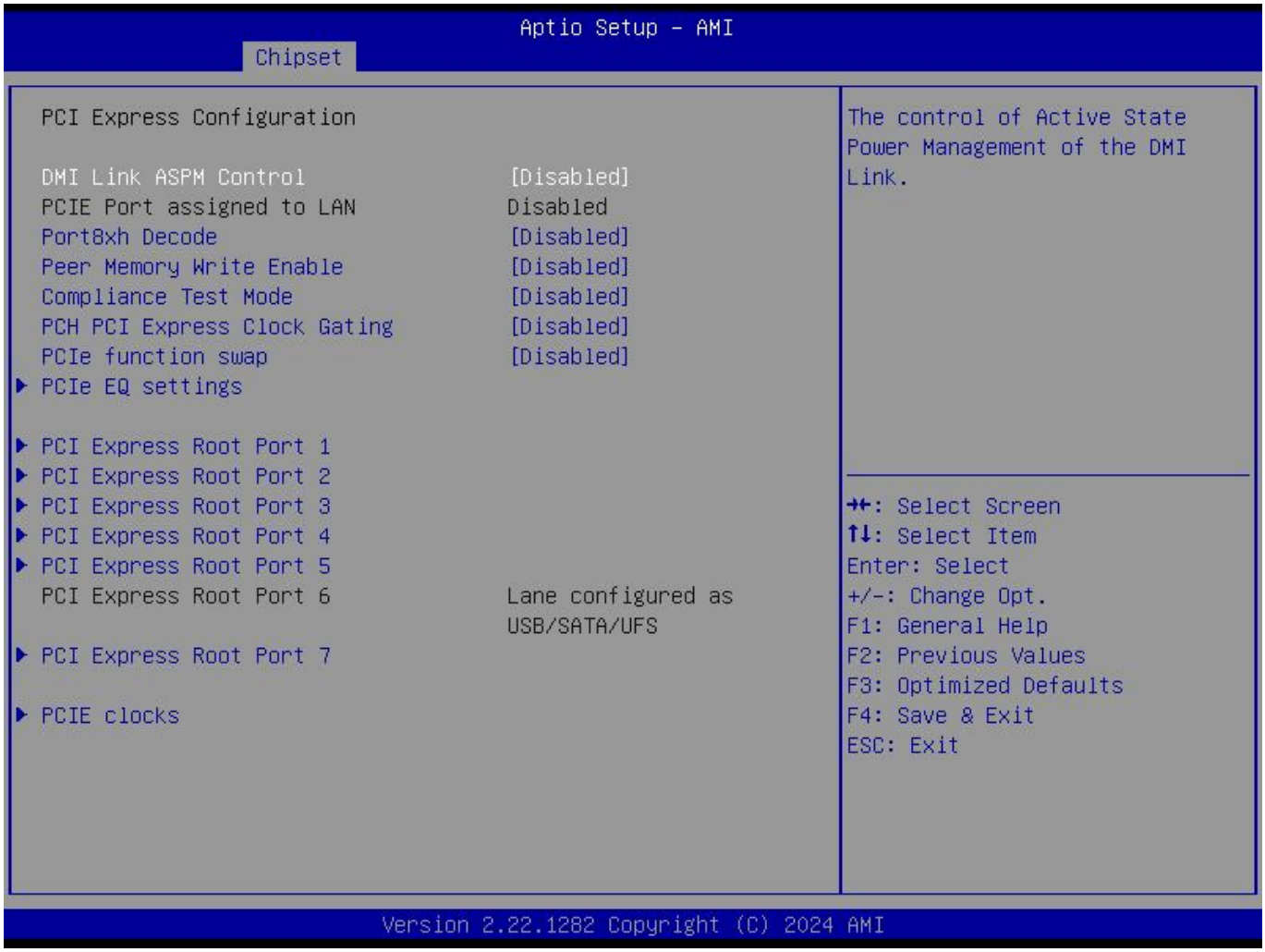
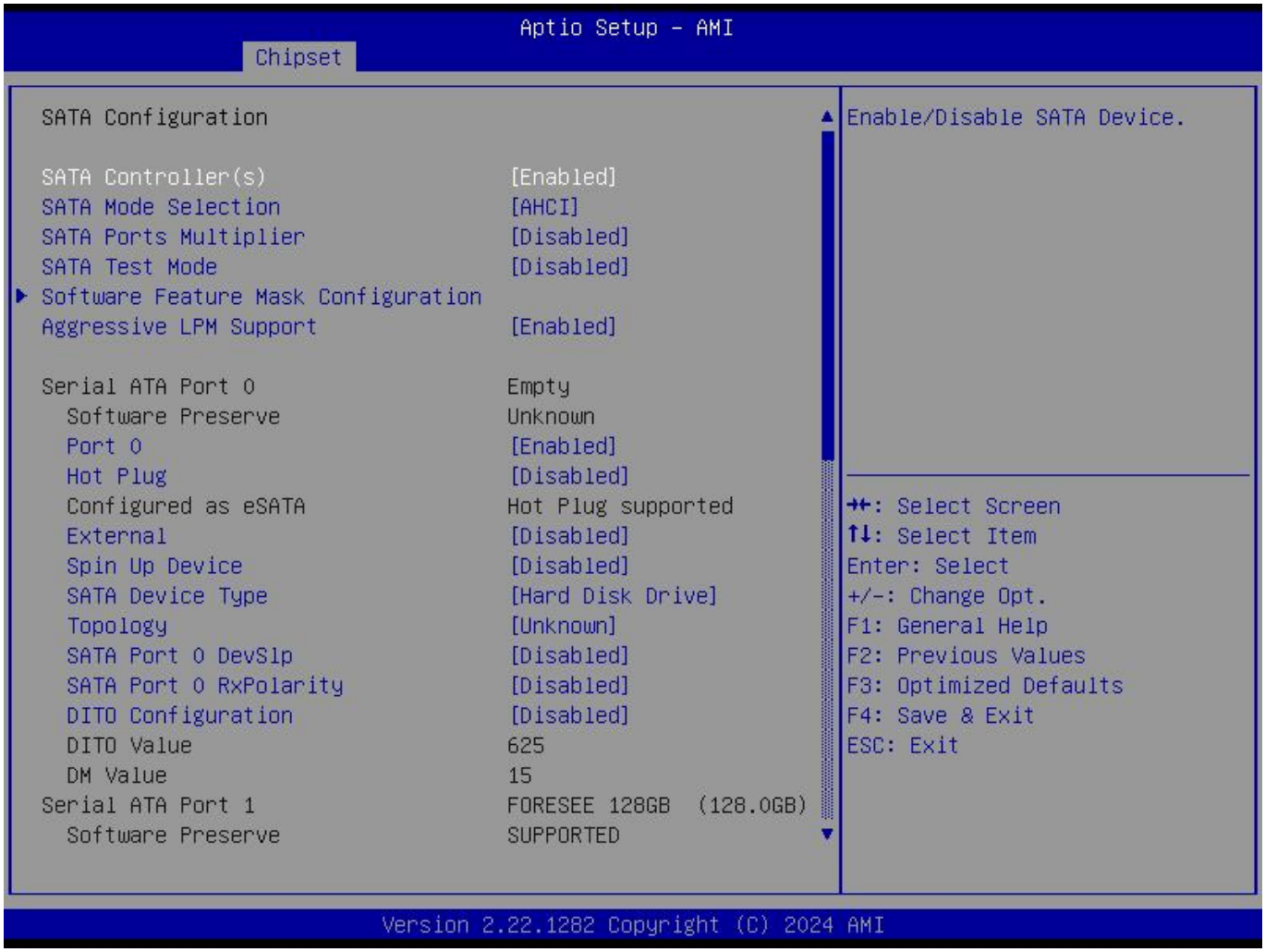
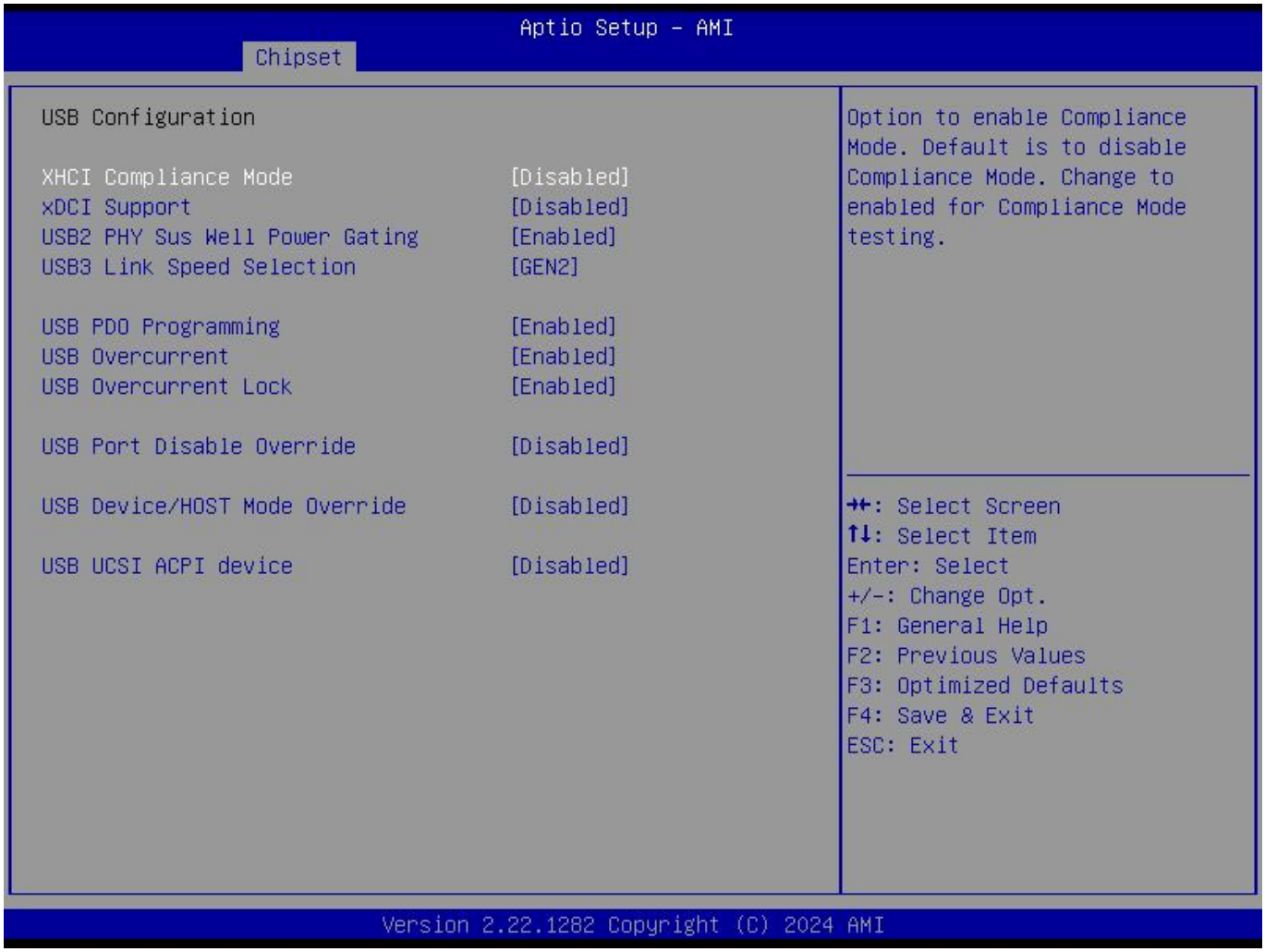


▶SATA And RST Configuration

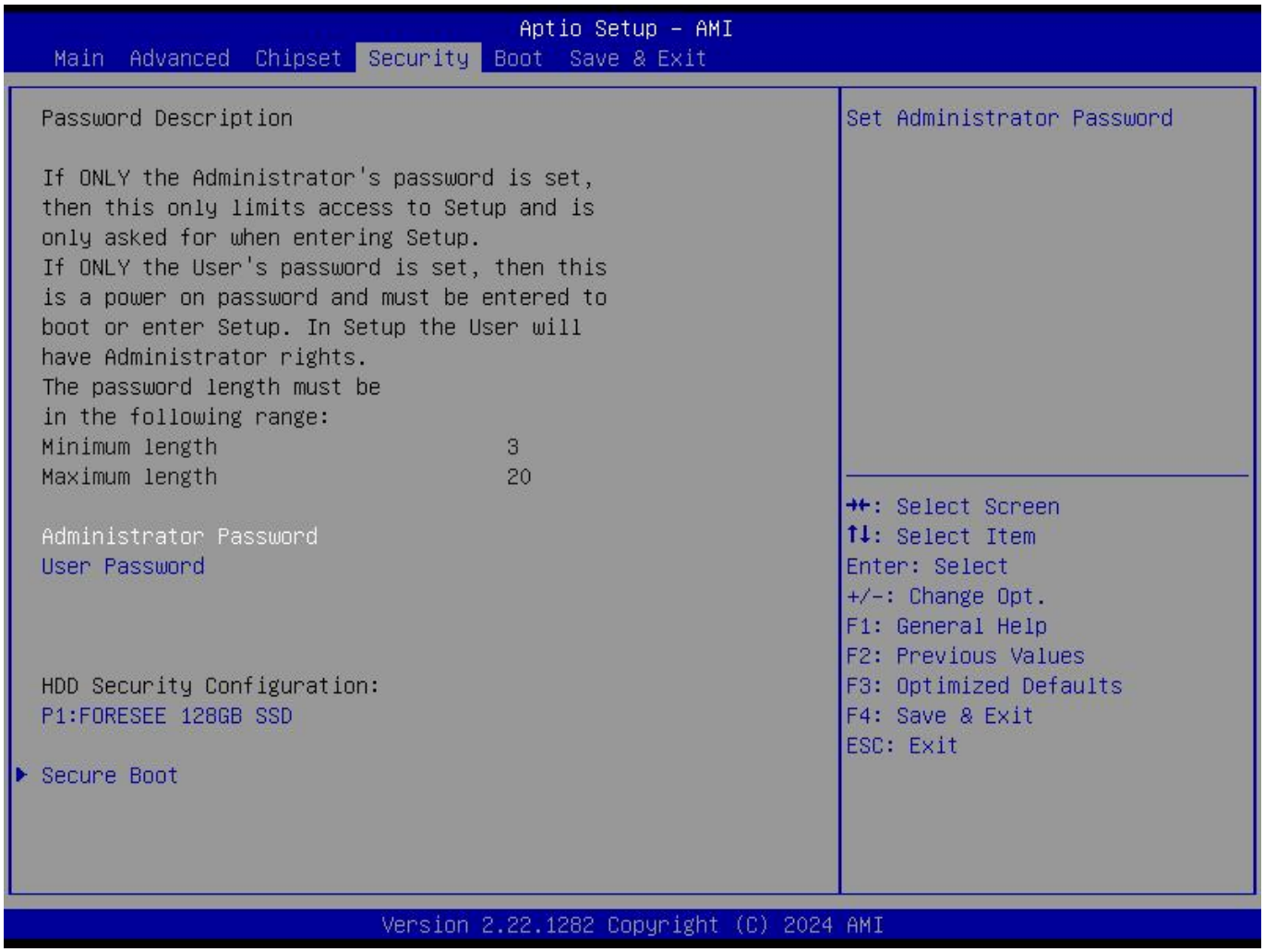
SATA hard disk and fast storage configuration, enter this sub-menu, there will be related settings of the hard disk.



▶USB Configuration


Aptio Setup - AMI
Chipset
USB Configuration
XHCI Compliance Mode [Disabled]
xDCI Support [Disabled]
USB2 PHY Sus Well Power Gating [Enabled]
USB3 Link Speed Selection [GEN2]
USB PDO Programming [Enabled]
USB Overcurrent [Enabled]
USB Overcurrent Lock [Enabled]
USB Port Disable Override [Disabled]
USB Device/HOST Mode Override [Disabled]
USB UCSI ACPI device [Disabled]
Option to enable Compliance Mode. Default is to disable Compliance Mode. Change to enabled for Compliance Mode testing.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1282 Copyright (C) 2024 AMI

3.2.5 Security menu



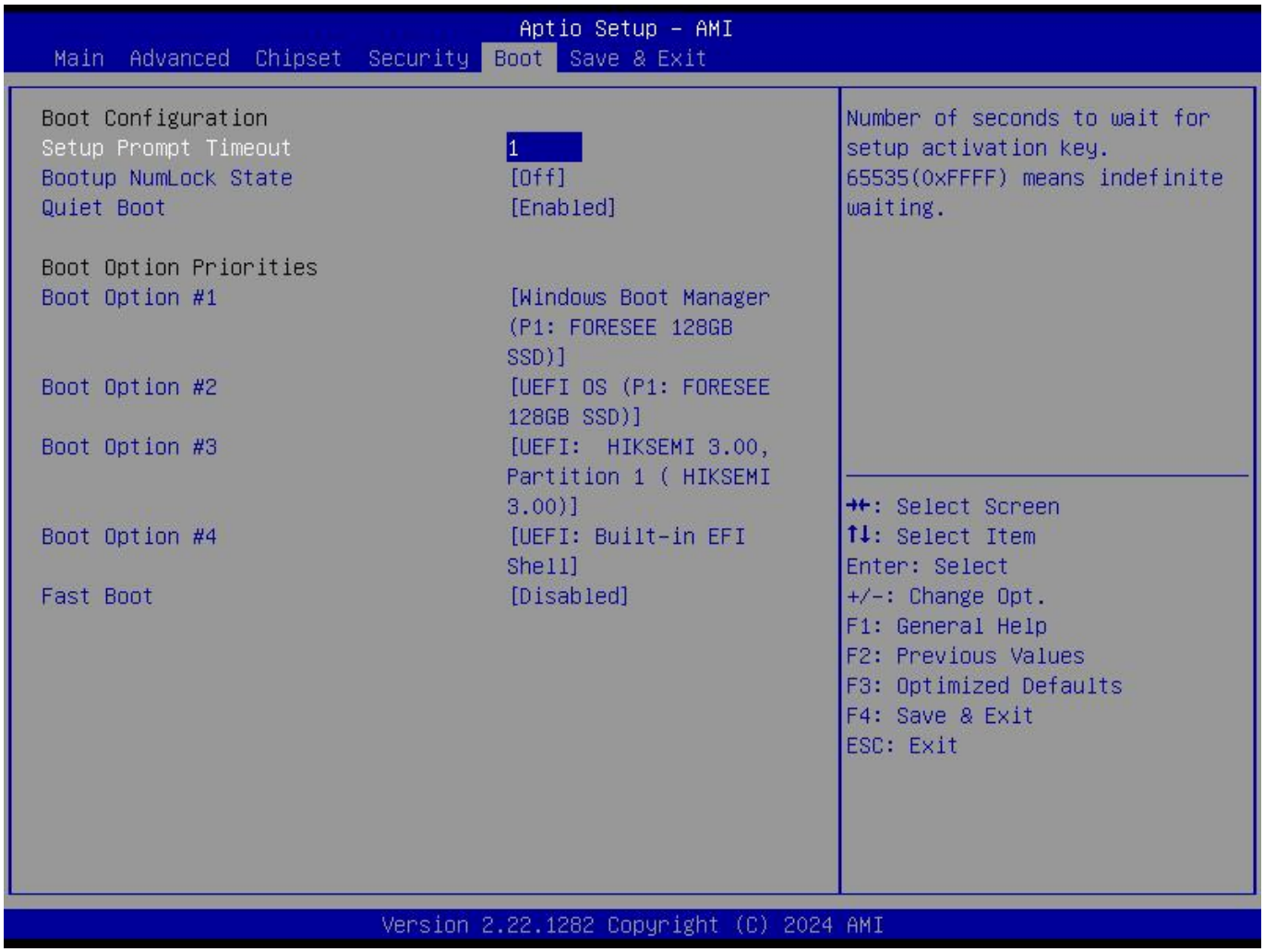
Administrator Password

This item sets the information of the administrator password.

User Password

This item sets the information of the normal user password.

3.2.6 Boot menu



Setup Prompt Timeout

Setup prompts for waiting time. This option is to set the time to wait for the Del key to enter the BIOS setup after booting.

Bootup NumLock State

Set the state of the small numeric keypad at startup.

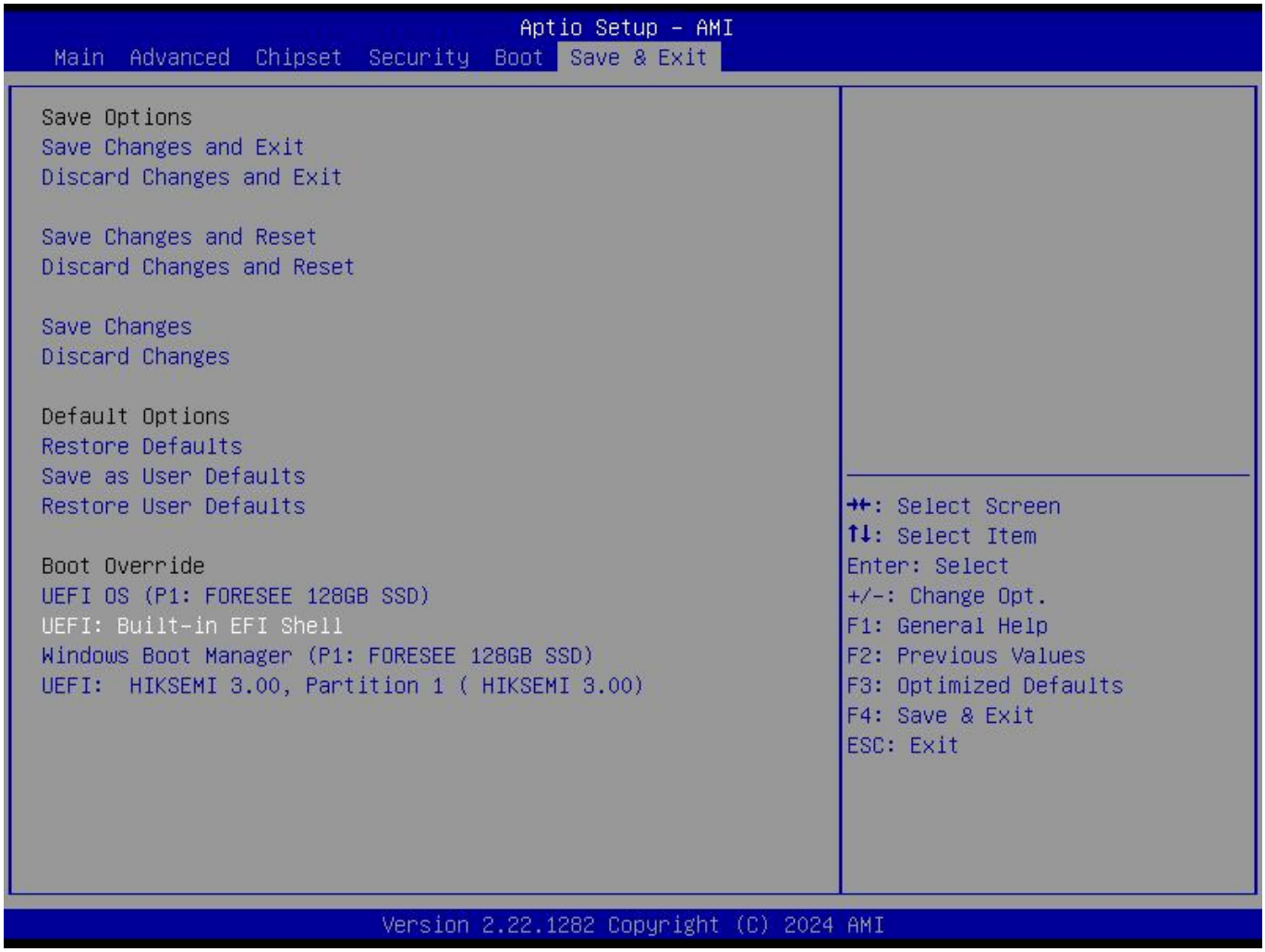
Quiet Boot

Switch full screen logo control

Fast Boot

Turn the quick start function on or off. When set to "Enabled", the system will skip some detection items and reduce the startup time.

3.2.7 Save & Exit menu



Save changes and Exit;

This item enables you to save the changes that you have made and exit.

Discard Changes and Exit;

This item enables you to discard the changes that you have made and exit.

Save Changes and Reset;

This item enables you to save the changes that you have made and reset.

Discard Changes and Reset;

This item enables you to discard the changes that you have made and reset.

Save Changes;

This item enables you to save the changes that you have made.

Discard Changes;

This item enables you to discard the changes that you have made.

Restore Defaults;

This item enables you to restore the system defaults.

Save as User Defaults;

This item enables you to save the changes as user defaults that you have made.

Restore User Defaults;

This item enables you to restore the user defaults.

3.3 Updating the BIOS

The BIOS (Basic Input and Output System) Setup Utility displays the system's configuration status and provides you with options to set system parameters. The parameters are stored in battery-backed-up CMOS RAM that saves this information when the power is turned off. When the system is turned back on, the system is configured with the values you stored in CMOS.

The BIOS provides the underlying driver for hardware resources and is the bridge between hardware and operating system. Now hardware and various applications are constantly updated. When your system encounters problems, such as the system does not support the latest published CPU, you need to upgrade your BIOS.

NOTE:

1. Only upgrade the BIOS if you encounter problems and need to.
2. To upgrade the BIOS, please use the BIOS read/write program attached to our driver CD or download the updated version of the program from the relevant website.
3. Do not turn off the power or reboot the system during the upgrade process, so your BIOS data will be damaged and the system may not boot.
4. After the refresh is complete, you need to manually optimize the LOAD Default.
5. To prevent accidents, please backup the current BIOS data first.

CHAPTER 4

SYSTEM RESOURCE

4.1 CAN

This section provides the specifications of all JHCTECH CAN functions and structures. All APIs use the naming convention jhctech_xxx specific to below table:

ID	Function Name
1.1	jhctech_init
1.2	jhctech_Close
1.3	jhctech_GetComMessage
1.4	jhctech_Receive
1.5	jhctech_SendDataFrame
1.6	jhctech_SendRemoteFrame
1.7	jhctech_SetGpioForAll
1.8	jhctech_SetGpioForOne
1.9	jhctech_ReadCom
1.10	jhctech_ReadOneGpio
1.11	jhctech_GetBaudRate
1.12	jhctech_SetBaudRate
1.13	jhctech_SetFilter
1.14	jhctech_Reset
1.15	jhctech_Version
2.1	jhctech_CheckUartError
2.2	jhctech_CheckCan0Error
2.3	jhctech_CheckCan1Error

jhctech_Init

PORT jhctech_init(int idx, int rate, int databits, int stopbits, int parity);

Function: Open the serial port and initialize it.

Parameters:

[in] idx : Port number

[in] rate : Baud rate

[in] databits : Data bits

[in] stopbits : Stop bits

[in] parity : Parity test

Return Value:

If the function succeeds ,return the Serial port file handle ,if the function fails , return value is less then zero.

jhctech_Close

void jhctech_Close(PORT COM);

Function: Close the serial port.

Parameters:

[in] COM: Serial port file handle

Return Value:

This function did not return.

jhctech_GetComMessage

int jhctech_GetComMessage(PORT COM, uint8_t* data, int len);

Function: Read message from serial port .

Parameters:

[in] COM : Serial port file handle

[out] data : Store data read from the serial port

[in] len : Number of bytes read from data

Return Value:

If there is a error in reading data , return -1 ;otherwise ,return the number of bytes read .

jhctech_Receive

void jhctech_Receive(Canbus_msg can, uint8_t* Message , int len);**

Function: Convert the infomation received by the serial port into the corresponding CAN structure.

Parameters:

[out] can : The structure that receives CAN data

[in] Message : Data received through serial port

[in] len : Data length

CAN frame structure:

```
typedef struct _Canbus_msg {
    struct _Canbus_msg* Next;
    uint16_t canStart;
    uint8_t canPort;
    uint32_t canId;
    uint8_t dataLength;
    uint8_t data[8];
    uint8_t cr;       //Check code
}Canbus_msg;
```

Return Value:

The function does not return a value.

jhctech_SendDataFrame

int jhctech_SendDataFrame(PORT COM, char canStart, uint8_t canPort, uint32_t canId, uint8_t* data, int data_len);

Function: The function is send data frame.

Parameters:

[in] COM : Serial port file handle

[in] canStart : Flag for the start of data frame

[in] canPort : CAN port for communication

[in] canId: The ID of the CAN frame

[in] data : The data of the CAN frame

[in] len : The length of the data

Return Value:

If the data frame is successfully send , return 0 ; Otherwise , return -1.

jhctech_SendRemoteFrame

int jhctech_SendRemoteFrame(PORT COM, char canStart, uint8_t canPort, uint32_t canId, uint8_t dlc);

Function: The function is remote data frame.

Parameters:

[in] COM : Serial port file handle

[in] canStart : Flag for the start of data frame

[in] canPort : CAN port for communication

[in] canId: The ID of the CAN frame

[in] dlc : Control code

Return Value:

If the remote frame is successfully send , return 0 ; Otherwise , return -1.

jhctech_SetGpioForAll

int jhctech_SetGpioForAll(PORT COM, uint8_t level);

Function: Set up the singlr gpio for the serial port , return -1 for error , 0 for correct .

Parameters:

[in] COM : Serial port file handle

[in] level : The level of entire serial port

Return Value:

If the serial port is successfully set ,return -1 for error , 0 for crrect .

jhctech_SetGpioForOne

int jhctech_SetGpioForOne(PORT COM, int pin, int level);

Function: Set up the singlr gpio for the serial port , return -1 for error , 0 for correct .

Parameters:

[in] COM: Serial port file handle

[in] level : The level of entire serial port

Return Value:

If the singlr gpio for the serial port is successfully set ,return -1 for error , 0 for crrect .

jhctech_ReadCom

int jhctech_ReadCom(PORT COM ,uint8_t *com_level);

Function: Obtain the level status of th entire serial port .

Parameters:

[in] COM : Serial port file handle

[out] com_level : The read serial port level

Return Value:

Return a negative number to indicate an error , otherwise return 0 . If return to -1 , sending command failed . If return to -2 , receiving data failed . If return to -3 , it indicates that is not a CAN frame.

jhctech_ReadOneGpio

int jhctech_ReadOneGpio(PORT COM, int pin , uint8_t * pin_level);

Function: Open the serial port and initialize it.

Parameters:

[in] COM: Serial port file handle

[in] pin : Pin to be read (0-7).

[out] pin_level : The read pin level

Return Value:

Return a negative number to indicate an error , otherwise return 0 . If return to -1 , sending command failed . If return to -2 , receiving data failed . If return to -3 , it indicates that is not a CAN frame.

jhctech_GetBaudRate

int jhctech_GetBaudRate(PORT COM, uint8_t can_port , uint8_t * baud);

Function: Obtain the baud rate.

Parameters:

baud rate	code
10k	0
20k	1
50k	2
100k	3
125k	4
250k	5
500k	6
800k	7
1M	8

[in] COM : Serial port file handle

[in] can_port: CAN port of obtain baud rate

[out] baud : The read baud rate code from CAN

Return Value:

Return a negative number if an error occurs, otherwise return the corresponding baud rate code. If return to -1 , sending command failed . If return to -2 , receiving data failed . If return to -3 , it indicates that is not a CAN frame.

jhctech_SetBaudRate

int jhctech_SetBaudRate(PORT COM, uint8_t can_port, uint8_t baud);

Function: Set the baud rate.

Parameters:

[in] COM: Serial port file handle

[in] can_port : CAN port of obtain baud rate

[in] baud : The baud rate code to be set(0-8)

Return Value:

Return a negative number if an error occurs, otherwise return 0.If the error code is -1 , the table name baud rate code is not within the range . If the error code is -2 , send data failed .

jhctech_SetFilter

int jhctech_SetFilter(PORT COM, uint8_t can_port, uint8_t idType, uint8_t index, uint8_t mode, uint32_t id1, uint32_t id2);

Function: Set hardware filtering.

Parameters:

[in] COM : Serial port file handle

[in] can_port : CAN port of set filtring

[in] idType : ID type , FDCAN_STANDARD_ID or FDCAN_EXTENDED_ID

[in] index : If ID type is FDCAN_STANDARD_ID , then it is 0-27 . If ID type is FDCAN_EXTENDED_ID ,then it is 0-7.

[in] mode : Filter mode

[in] id1 : The fist ID of the filtering condition.

[in] id2 : The second ID of the filtering condition.

Filter Mode:

```
#define FDCAN_FILTER_RANGE          0
#define FDCAN_FILTER_DUAL           1
#define FDCAN_FILTER_MASK           2
#define FDCAN_FILTER_RANGE_NO_EIDM  3
```

TD Type:

```
#define FDCAN_STANDARD_ID    0
#define FDCAN_EXTENDED_ID    1
```

Return Value:

If filter is successfully set , return 0 , otherwise return -1 .

jhctech_Reset

int jhctech_Reset(PORT COM);

Function: MCU restarts .

Parameters:

[in] COM: Serial port file handle

Return Value:

Returns 0 if successful, otherwise returns -1.

jhctech_Version

int jhctech_Version(PORT COM, int* major, int* minor);

Function: Obtain the software version number .

Parameters:

[in] COM: Serial port file handle

[in] major : Main version number

[in] minor : Minor version number

Return Value:

Returns 0 if successful. The version is major and minor. Otherwise, return a negative number . If return to -1 , sending command failed . If return to -2 , receiving data failed . If return to -3 , it indicates that is not a CAN frame.If return to -4 , the fame is not version information .

ERROR FRAME

UART error code:

```
#define  UART_ERROR_NONE   (0x00000000U)  /*!< No error      */
#define  UART_ERROR_PE     (0x00000001U)  /*!< Parity error  */
#define  UART_ERROR_NE     (0x00000002U)  /*!< Noise error   */
#define  UART_ERROR_FE     (0x00000004U)  /*!< Frame error   */
#define  UART_ERROR_ORE    (0x00000008U)  /*!< Overrun error */
#define  UART_ERROR_DMA    (0x00000010U)  /*!< DMA transfer error */
#define  UART_ERROR_RTO    (0x00000020U)  /*!< Receiver Timeout error */
```

FDCAN error code :

```
/*!< No error                                    */
#define  FDCAN_ERROR_NONE                ((uint32_t)0x00000000U)
/*!< Timeout error                               */
#define  FDCAN_ERROR_TIMEOUT             ((uint32_t)0x00000001U)
 /*!< Peripheral not initialized                 */
#define  FDCAN_ERROR_NOT_INITIALIZED ((uint32_t)0x00000002U)
/*!< Peripheral not ready                        */
#define  FDCAN_ERROR_NOT_READY           ((uint32_t)0x00000004U)
/*!< Peripheral not started                      */
#define  FDCAN_ERROR_NOT_STARTED         ((uint32_t)0x00000008U)
/*!< Mode not supported                          */
#define  FDCAN_ERROR_NOT_SUPPORTED       ((uint32_t)0x00000010U)
/*!< Parameter error                             */
#define  FDCAN_ERROR_PARAM               ((uint32_t)0x00000020U)
/*!< Pending operation                           */
#define  FDCAN_ERROR_PENDING             ((uint32_t)0x00000040U)
/*!< Message RAM Access Failure                  */
```

```
#define     FDCAN_ERROR_RAM_ACCESS          ((uint32_t)0x00000080U)
/*!< Put element in full FIFO               */
#define     FDCAN_ERROR_FIFO_EMPTY          ((uint32_t)0x00000100U)
/*!< Get element from empty FIFO            */
#define     FDCAN_ERROR_FIFO_FULL           ((uint32_t)0x00000200U)
```

jhctech_CheckUartError

uint32_t jhctech_CheckUartError(uint8_t* msg, int len);

Function: Check for erroneous frames .

Parameters:

[in] msg : Data received through serial port

[in] len : Data length

Return Value:

If there is an error frame , return an error code . Otherwise return 0.

jhctech_CheckCan0Error

uint32_t jhctech_CheckCan0Error(uint8_t* msg, int len);

Function: Check for erroneous frames .

Parameters:

[in] msg : Data received through serial port

[in] len : Data length

Return Value:

If there is an error frame , return an error code . Otherwise return 0.

jhctech_CheckCan1Error

uint32_t jhctech_CheckCan1Error(uint8_t* msg, int len);

Function: Check for erroneous frames .

Parameters:

[in] msg : Data received through serial port

[in] len : Data length

Return Value:

If there is an error frame , return an error code . Otherwise return 0.

4.2 DIO

jhctech_SetGpioForAll

int jhctech_SetGpioForAll(PORT COM, uint8_t level)

Parameters:

@brief Set the entire serial port gpio , return -1 for error , 0 for correct .

@param [in] COM : Serial port file handle

@param [in] level : The level of entire serial port

Return Value:

@return If the serial port is successfully set ,return -1 for error , 0 for crrect .

jhctech_SetGpioForAll

int jhctech_ReadCom(PORT COM , uint8_t *com_level)

Parameters:

@brief Obtain the level status of th entire serial port .

@param [in] COM : Serial port file handle

@param [out] com_level : The read serial port level

Return Value:

@return Return a negative number to indicate an error , otherwise return 0 .If return to -1 , sending command failed . If return to -2 , receiving data failed .

If return to -3 , it indicates that is not a CAN frame.